Application note

ARTEMiS-SSN switch models

Version: 1.0.1
Last update: 2018-06-14
Author: Christian Dufour

Opal-RT Technologies

Contents

Document revision history

v 1.0	First version	June 5, 2018
v1.0.1	Added swithed iteration options	June 14, 2018

1. Executive summary

This document objective is to explain the various methods used to simulate switches in SSN including Time-Stamped Bridge (TSB) and its variants.

The other aspect of this topic relates to specialty methods for switches, namely: TSB, TSB with real-diodes (TSB-RD), Inlined Voltage Ìnverter Compensation (IVIC), Inlined Thyristor Valves compensation (ITVC) and iterative switch (iSWITCH) methods

In summary:

-For small inverter models, TSB and IVIC methods are good enough.

-IVIC is recommended for inverter models with limited PWM frequency (under 10% of simulation sampling frequency).

-For larger more realistic cases involving many inverter not easily decouplable, it is recommended to use TSB-RD in conjunction with SSN. IVIC is also good in this.

-ITVC is recommended for thyristor applications like HVDC, SVC and similar converters.

-iSWITCH methods are best advised in general topologies, except for classic inverter cases where TSB, IVIC, TSB-RD are better because of interpolation, a feature than iSWITCH does not have.

2. Software Requirement

Table 1 List of Software required

Software Names	Versions
MATLAB	R2015a
ARTEMiS	7.2.2 (R2015a)

3. SSN switch methods and models

Several methods and models for switch exists in ARTEMiS and SSN: TSB, TSB with real-diodes, Inlined Voltage Ìnverter Compensation (IVIC) and Inlined Thyristor Valves compensation (ITVC) methods.

TSB are interpolated switching function based (2-level and 3-level NPC) inverters models that do not have any binary switch (or SPS switch). The importance of this is that TSB do not contribute to precalculation of switch permutations in ARTEMiS and/or SSN. Equivalent switching accuracy is 10 nanoseconds (with Time-Stamped I/O or RT-Events). Disadvantages are the requirement of (sometimes) large snubbers in high-impedance mode.

TSB with real-diode (TSB-RD) are TSB with real SPS diode for the anti-parallel diode modeling. They are more accurate in high-impedance mode than TSB but they will count in the switch permutation pre-calculation. They are better used in conjunction with SSN therefore.

IVIC is an SSN switch algorithm for 2-level inverter with interpolation. It is as accurate as TSBs but as no input-output delay and more stable in high-impedance mode than TSB. One disadvantage is that the PWM frequency must be strictly limited to $F_s/10$ (F_s is the simulation sapling frequency or $1/T_s$) otherwise it may not work at all. TSB are better at this as there interpolation method will simply filter out the PWM components of simulation when PWM frequency approaches F_s.

ITVC is a switching algorithm for thyristor valves only. Using interpolation methods, ITVC accuracy is similar to IVIC and TSB (only limited by I/O sample time, i.e 5 or 10 ns typically).

The word Inlined of IVIC and ITVC means that the methods are highly efficient. They are inlined in the code and they computational cost is close to 0. The methods are not based on successive interpolation/extrapolation of switch events like in old generations of ARTEMiS.

iSWITCH are SSN iterative switch models that can be used for all switching devices like diode, thyristor, IGBTs, IGBT/diode, MOSFET, GTO, etc…

Figure 2 summarize the relative advantage and disadvantages of these methods.

	type	+	-
TSB	block	PWM interpolation to Fs No memory impact	High-impedance and natural rectification mode is complex to set-up Possible instability if DC bus voltage goes negative
TSB real-diode (TSB-RD)	block	PWM interpolation to Fs Easier high-impedance support Better support of DC bus faulting. Support parallelization of inverters Can be made immune to involuntary cross-talk.	Counts for memory pre-calculation as SPS switches. This problem is solved by the use of SSN.
IVIC	SSN embedded	PWM interpolation to Fs/10 Better fault capability than TSB	Only for 2-level inverter. An IVIC 3-level NPC inverter exists but somehow limited in usage.
ITVC	SSN embedded	Very accurate, Time-Stamp compatible (I/O or RT-Events)	Only for thyristor
iSWITCH	SSN embedded	Most accurate method, except in PWM application where TSB, TSBRD and IVIV can be better.	iSWITCH model do not have interpolation capability, except thyristor ITVC. Iterations can slow down simulation Complex SSN node set-up

Table 2: List of switching methods and algorithms in ARTEMiS and SSN.

3.1 TSB

TSB are probably the most widely used model in Opal-RT simulators. TSB are interpolated switching function and can only be used to simulate certain switch structures like 2-level inverters and 3-level inverters.

The working principle of TSB is to act like a voltage router to the load and a current router to the DC link.

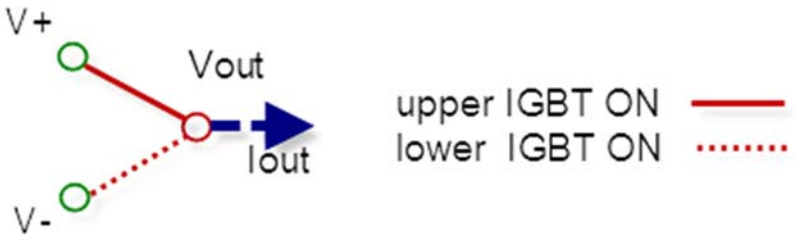

Figure 1: Simplified TSB principle in active mode

This routing is made with a fixed causality: DC bus input voltage (V+) is forced onto the load if the upper IGBT gate is ON; output load current (Iout) is injected on the upper DC bus terminal if the upper IGBT gate is ON.

For the load voltage, it is also computed at each time step and proportional to the gate signal time. If the upper gate is ON for 50% of the time step (case without deadtime), then the load voltage, for that time step will be forced to 50% of the DC bus voltage. This is called Time Step Based Averaging Modeling and is different than the typical 'average model' concept.

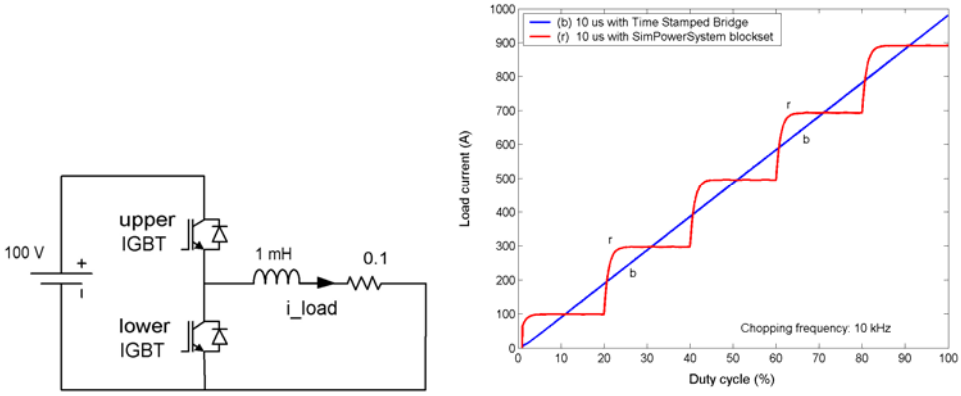

Figure 2: PWM duty-cycle scan of a simple chopper: effect of interpolation

The effect of TSB interpolation can be viewed in the figure above. It shows the load current as a function of PWM duty cycle for a simple inverter. In the test, Ts=10µs and the PWM frequency equal 10 kHz, with is 10% of the simulation sampling frequency of 100 kHz. Gating can come from interpolation-capable RT-Events or from Time-Stamped Digital Input (TSDIN) without difference.

3.1.1 Deadtime

Deadtimes are short delays that inverter controllers insert in the firing sequence to avoid that both IGBTs are ON at the same time. This causes the inverter to have small times where both IGBT are OFF; during that time, with continuously conducting load, anti-parallel diodes turn ON for a that time. Opal-RT TSB can take into account deadtimes using a small piece of logic based on reality: one of the 2 anti-parallel diode turns ON instantaneously during deadtime, applying either V+ or V- like IGBTs, and the current direction only determines which anti-parallel diode turns ON.

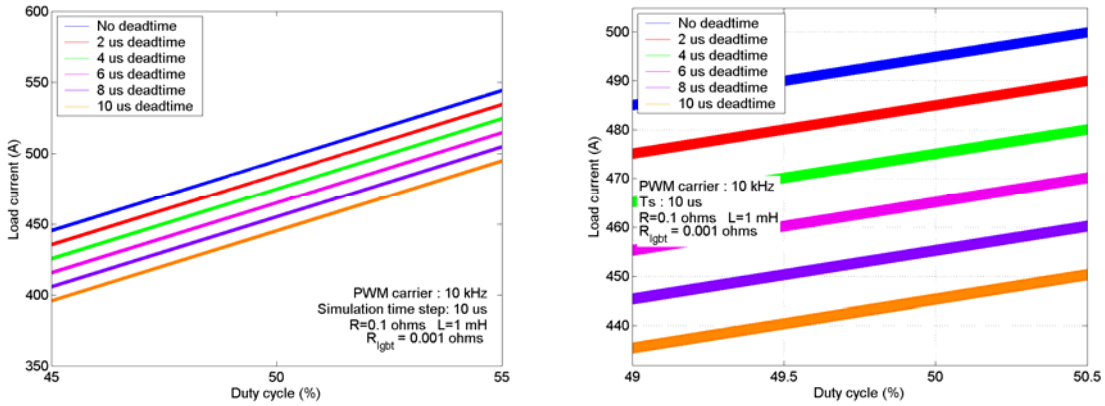

Figure 3: Deadtime effect on TSB-simulated chopper.

The figure above displays a test made with the same 10kHz chopper as before. This time, we add small amount of deadtime and we can observe that the current response drops smoothly as it is supposed to do in theory. It is somewhat remarkable that Opal-RT TSB supports deadtimes much shorter than the simulation time step (as opposed to SPS switching function models as of 2018).

3.1.2 High-impedance mode

High-impedance model occurs in inverters when all IGBT gates are OFF and the current goes to zero. In that case, the inverter cease to be a 'voltage router' to the load and exhibits a high-impedance state.

Natural rectifying modes of inverter involve this high-impedance mode as phase turns in high-impedance alternatively.

With the TSB, this mode is supported with a null current feedback look with PI control. Since PI control equations are much similar to a series RC snubber, it is called 'RC snubber' in TSB dialog box. These snubbers requires some adjustments for stability purposes and readers are directed to the application note '***High-impedance snubber adjustments for ARTEMiS TSB***' to know more about it.

3.2 TSB with real diodes (TSB-RD)

TSB-RD are TSB in which all the snubber logic (i.e. PI control) of the high-impedance mode is made with real SPS diodes or a combination of thyristors (which are enablable diodes) and ideal switches. In the latter, the ideal switch is ON during active mode and the thyristor are activated (i.e. become equivalent to diodes) when IGBT pulses are turned OFF. This latter 3-switch topology has the advantage of adding absolutely no delays.

TSB with real-diode (TSB-RD) have all the functionalities of TSB but implement the high-impedance mode in much more natural way, i.e. with SPS switches. Note that TSB-RD still need RC snubbers (real ones this time) in many cases but they will typically be smaller in size (i.e. have a higher impedance).

The main advantage of TSB-RD is that they have a much better numerical behavior in many cases.

The main difference of TSB-RD is that they count in switch precalculations made by the ARTEMiS-SSN real-time solver. In SSN, this is absolutely NOT blocking as the TSB-RD can be put in different SSN groups.

3.2.1 Example with TSB-RD, SSN and DC-bus decoupling

In the complex drive of Fig. 4 below, several inverters are connected in parallel to obtain several power levels at the load. In HIL mode, the main difficulty of this model is that parallel inverter gating can have a small delay between them due to cabling or firing pulse unit tolerances (up to 200 ns). Deadtime is 3 µs. Several techniques are used to obtain an accurate simulation:

1- TSB-RD are used in the model

2- All rectifier-side and inverter-side 2-level inverters are isolated from each other by using the DC-bus capacitor delay method.

3- Because each 3-phase TSB-RD is modeled with 3x3=9 switches, each TSB-RD must be decoupled at the load and grid side also. This is done with using an SSN node at the interphase inductance connection point.

4- The interphase inductance impedance were lowered by adding a parallel resistance that limit the total impedance at 1 kHz ($R = 2 * \pi * 1000 * L$) to increase stability.

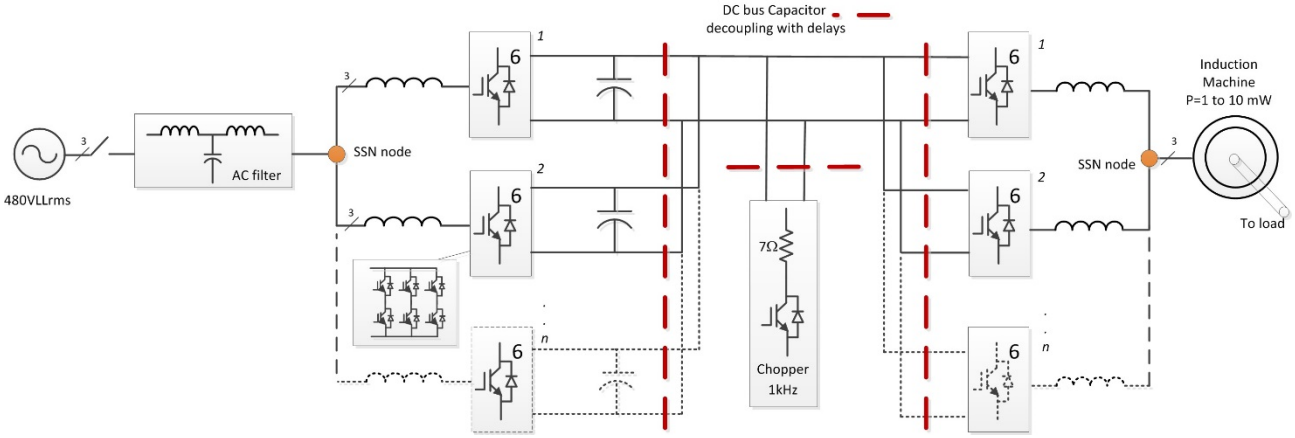

Figure 4: A complex and scalable AC-DC-AC motor drive

The technique used here are scalable in the sense that parallel inverters can be added (dashed in the image) to the model without impact on real-time simulation capability.

One of the major difficulty of this model can from the small gating delays (0-200 ns in spec) on the various parallel inverters that arises from the real Firing Pulse Unit of this device. This is a subtle but nevertheless existent advantage of TSB-RD over IVIC: it's easier to adapt to special conditions. In the case above, we has to modify the dead-time logic of the TSB-RD so that they all take identical current polarity at all time.

In another client case, TSB-RD had to be modify to filter out cross-talk between channels of different phases.

3.3 IVIC

IVIC (Inlined Voltage Inverter Compensation) is an embedded SSN method aimed at compensating 2-level inverters (and 3-level NPC) like TSB but without input-output delays.

The SSN demo ***ARTEMiS-SSN Inlined Time-Stamped Bridge in 2-level VSC-based HVDC applications using IVIC algorithm(SSN***) shows an actual client case where the TSB delays were causing some voltage and current fluctuations. The use of SSN-IVIC algorithm made these oscillation disappears. In the figure above, one can observe the use of the 'ARTEMiS SSN Inlined TSB' block which is required for SSN-IVIC usage.

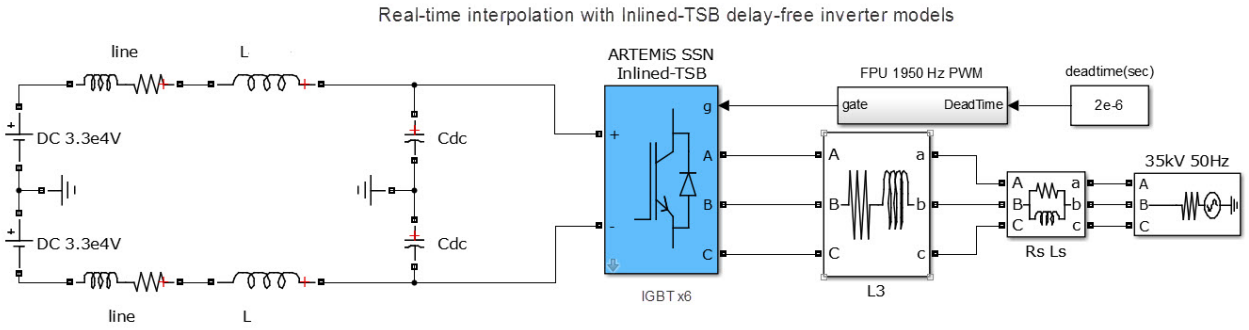

Figure 5: VSC-based HVDC link using SSN-IVIC method.

One disadvantage of the IVIC is that PWM frequency has to be limited to $\frac{1}{10T_s}$ typically.

3.4 ITVC

ITCV (Inlined Thyristor Valve Compensation) is an embedded SSN method aimed at compensating thyristor firing delays with regards to the sample time frame of the simulator. It is useful to avoid uncharacteristic current jitter in HVDC or SVC applications.

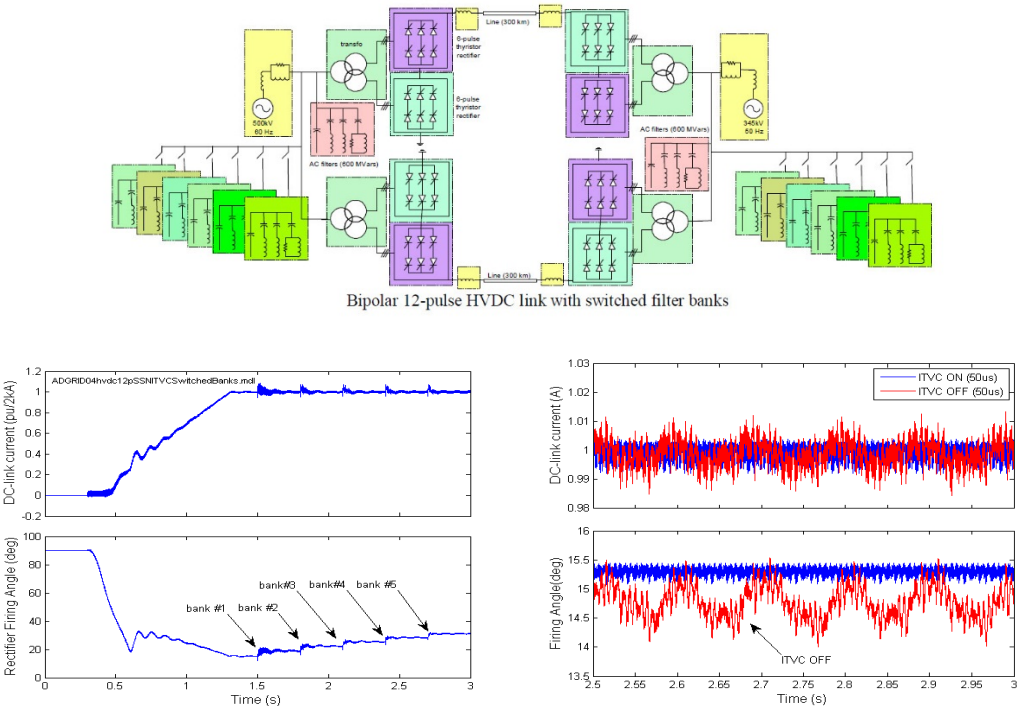

Figure 6: Bipolar HVDC link with switched filter and effect of ITVC algorithm.

This can be seen in SSN SVC demo ***Static VAR compensator +300/-100 Mvars, thyristors-based*** or the SSN HVDC demo ***Bipolar 12-pulse HVDC link with switched filter banks.*** The latter is depicted in figure xx above and show improved DC current and firing angle response with ITVC algorithm. The noise seen on the curves 'ITVC OFF' is simply due to the sampling effect of thyristor gating, not because of controller issues.

ITVC method uses regular SPS thyristor blocks, as is. For ITVC to work, the thyristor gate must be driven by a Time-Stamped Digital Input signal (HIL) or RT-Events signals (offline).

3.5 iSWITCH

iSWITCH is an embedded SSN method aimed at making accurate simulation of any power converters using iterative methods.

Historically, most real-time simulators have avoid iteration to keep up with computation performance. The old EMTP did not iterate either for the same reason in part. With modern CPU technology and speed, iterations can be done in real-time, as in HYPERSIM and SSN.

There are many cases where iteration are required which are typically converters with fast current loop.

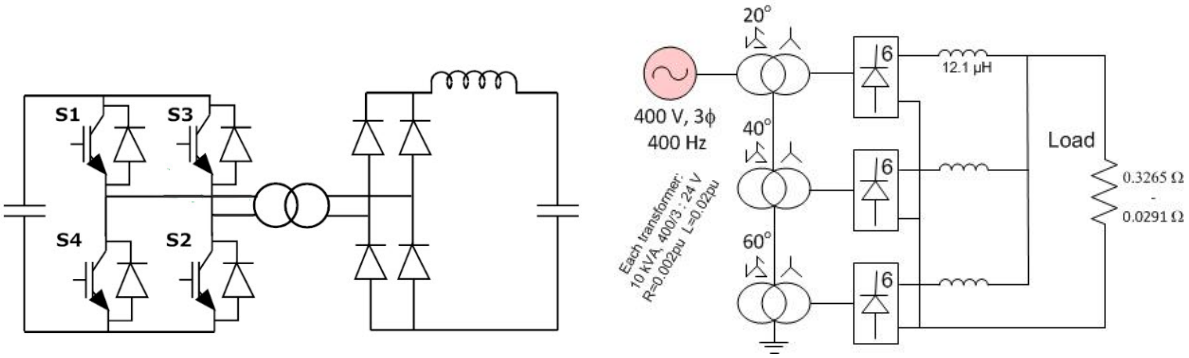

Figure 7: HVDC DC-DC converter (left) and Aerospace-type 18-pulse rectifier (right)

The two cases above, left, an HVDC DC-DC converter circuit, right, an 18-pulse rectifier used in aerospace applications, have very fast switching actions involving current loop going thought the transformer. They can only be simulated accurately using SSN iSWITCH method at time steps compatible with real-time simulation. The user is invited to look into the ***SSN Iterative Model*** section to try the demos.

The SSN iSWITCH method is implemented in SSN using regular SPS switches and detected as 'Iterative' by their special SSN group characteristics, that is: 1) the switch is alone inside a SSN group with parallel R only if wanted and 2) interfaced with V-type NIB. (NIBs, Nodal Interface Blocks, are SSN nodes in the SPS model). In doubt, the user should check the Simulink printout to make sure that iSWITCH have been detected as such. Below is the listing for the 6-pulse aerospace rectifier demo using 6 iterative diodes.

```
...
ARTEMIS-SSN: approx. memory required: 0.004312 Mb (including nodal matrix)
SSN group info
Group 1 : 2 states, 3 inputs, 6 outputs, 0 switches.
Group 2 : 9 states, 6 inputs, 9 outputs, 0 switches.
Group 3 : 0 states, 4 inputs, 3 outputs, 1 switches.(SSN Iterative switch group)
Group 4 : 0 states, 4 inputs, 3 outputs, 1 switches.(SSN Iterative switch group)
Group 5 : 0 states, 4 inputs, 3 outputs, 1 switches.(SSN Iterative switch group)
Group 6 : 0 states, 4 inputs, 3 outputs, 1 switches.(SSN Iterative switch group)
Group 7 : 0 states, 4 inputs, 3 outputs, 1 switches.(SSN Iterative switch group)
Group 8 : 0 states, 4 inputs, 3 outputs, 1 switches.(SSN Iterative switch group)
SSN nodal matrix is of rank 5 (0 % of zeros) (0 prefactorized col/rows)
...
```

The main advantage of the iSWITCH method is of course its great accuracy. One downfall is that it tend to create nodal matrices of larger size than normally required. iSWITCH do not make interpolation (with the exception of the thyristor)

3.5.1 iSwitch iteration control

The maximum number of iteration of iSWITCH model can be controlled from the ARTEMiS GUIde menu item: '**Maximum number of iteration (iMOV and iSWITCH)**'

(iMOV is an iterative MOV model of SSSN, not discussed here)

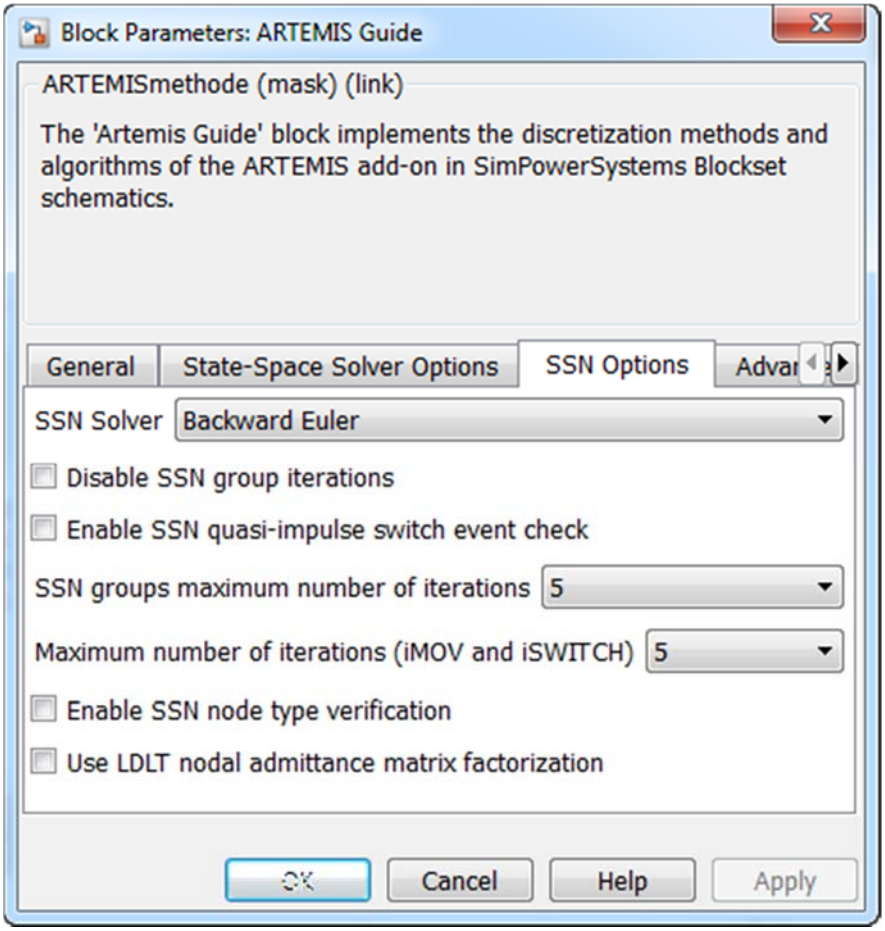

Figure 8. SSN solver option of ARTEMiS GUIde.

Other iteration options are NOT related to iSWITCH models. '**Disable SSN group iteration**' and '**Enable SSN quasi-impulse switch event check**' and '**SSN groups maximum number of iterations**' are 3 options related to switch calculation in normal SSN groups. SSN makes partial iterations by default inside each group. These are not real, global solver iteration but local iteration within each SSN group. They can improve the accuracy of SSN model by detecting instantaneous or quasi-instantaneous switch dependencies within a group.

4. References

[1] C. Dufour, J. Mahseredjian , J. Bélanger, "A Combined State-Space Nodal Method for the Simulation of Power System Transients", IEEE Transactions on Power Delivery, Vol. 26, no. 2, April 2011 (ISSN 0885-8977), pp. 928-935