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# Real-Time Simulation of Onboard Generation and Distribution Power Systems

Christian Dufour, Jean Bélanger, Simon Abourida

*Opal-RT Technologies inc.*
*1751 Richardson, #2525*
*Montreal (Quebec), H3K 1G6, Canada*
*{christian.dufour, jean.belanger, simon.abourida}@opal-rt.com*

## Keywords

Hardware-In-the-Loop simulation, Motor Drives, Power Electronics, Real-Time Simulation.

## Abstract

*This paper presents the RT-LAB Electrical Drive Simulator technology along with practical applications. The RT-LAB simulation software enables the parallel simulation of an electrical circuit on clusters of PC running QNX or RT-Linux operating systems at sample time below 10 μs. Using standard Simulink models including SimPowerSystems models, RT-LAB build computation and communication tasks necessary to effectively make parallel simulation of electrical systems with low cost off-the-shelf PC technology. To accommodate the high bandwidth of electrical systems, the RT-LAB Electrical Drive Simulator comes with special Simulink-based modeling tools, namely ARTEMIS and RT-Events that permits real-time simulation of electrical systems at practical time step of 10 us but with sub-μs equivalent precision through the use of interpolation techniques.*

## I. Introduction

Automatic code generation software such as Real-Time Workshop and Autocode has made it possible to build very powerful real-time simulators like RT-LAB without writing any code by hand. An engineer can now go directly from a Simulink or SystemBuild simulation to hardware implementation with minimal debugging time. Since the introduction of real-time simulation, two major applications have emerged: rapid prototyping of controllers and Hardware-in-the-Loop (HIL) testing of production-line controllers. In rapid prototyping, a controller is first modeled in Simulink and the model is then compiled to run on a specified target system allowing testing of the controller algorithm against a real plant. In HIL simulation testing of production-line controllers, the actual controller is tested against a simulated plant model running in the real-time simulator.

While controller rapid-prototyping is a well-established technique, the HIL plant simulation technique is more difficult to realize for electrical systems for several reasons. For example, electrical systems usually have a lot of working modes caused by switches. Electrical systems also tend to be "stiff" by nature, requiring very small time steps or variable-step solvers to achieve convergence and/or accuracy.

The last difficulty comes from the use of power electronic switching devices running at high commutation frequencies. Emulating an IGBT motor inverter requires sub-microsecond precision on the firing time. This is problematic in HIL simulation where current hardware can barely simulate the system at a 10 μs time step. For power network simulation, even such a small time step requires special solvers and interpolation techniques to ensure accurate results.

This paper introduces the RT-LAB Electric Engineering simulator. The paper describes the hardware and software solutions used with some example applications for HIL simulation of electrical systems and drives.

## II. The RT-LAB real-time simulator

The RT-LAB simulator is designed to make the real-time simulation of Simulink or SystemBuild models on clusters of standard Pentium-based multi-CPU PC. Exploiting simulation parallelism in electrical systems poses some challenges at the hardware level, again because of the high bandwidth of such systems. Exchanging data between parallel tasks must be done at small sample time with very low communication time and latency. RT-LAB enables sub-μs latency data exchange between CPUs running

in parallel in two main ways: multi-CPU and multi-computer task parallelisation.

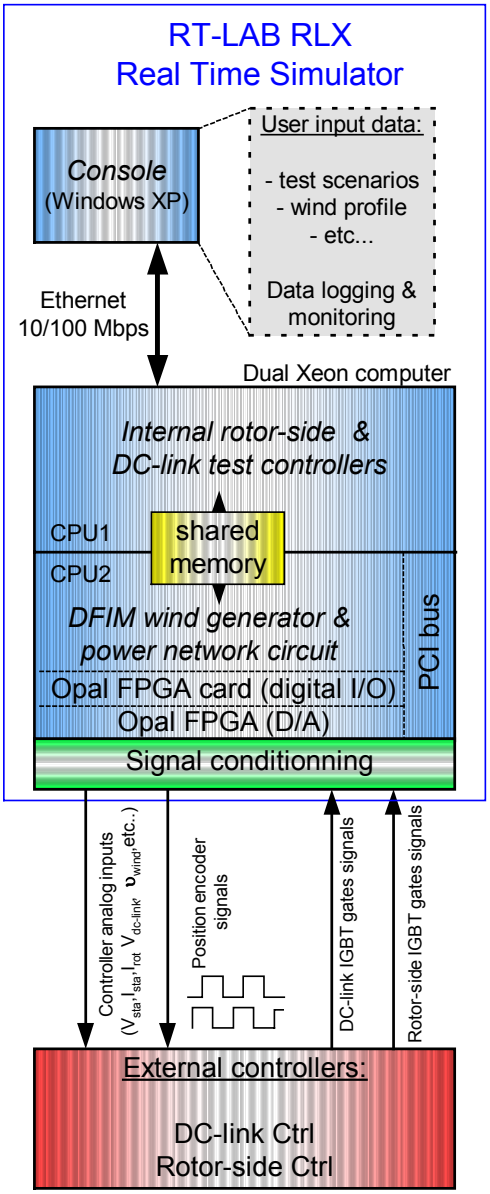



Fig. 1. Structure of the RT-LAB real-time simulator (wind generator model example)

The first method uses multi-CPU computer with shared memory. PC-based systems with Dual or Quad-Pentium processors are commercially available for this purpose. RT-LAB build parallel tasks from the original Simulink model and run them on each CPU of the multi-CPU computer. Data are exchanged though shared-memory that has ultra-low latency in the same order of the CPU system memory and thus permits the parallel simulation of electrical systems at time step below 10 µs. This method is shown in Fig. 1 for the doubly-fed induction generator for wind-turbine application. The figure shows a typical task separation on a dual-CPU computer: one CPU holds the plant model and I/O interface while the other CPU holds numerical version of the controllers.

The second method involves transmitting data between CPUs on separate PC through external communication links. To achieve this, RT-LAB uses an FPGA-based proprietary communication link called SignalWire™ capable to deliver up to 1.25 Gbit/s transfer rates, with a latency of 200 ns. With SignalWire links, one can run distributed simulations on PC-cluster at cycle times of less than 10 µs without data overruns.

The same FPGA board implements useful functionalities for hardware-in-the-loop testing of electrical systems. The RT-LAB platform is configured to be used with a supplied library of Simulink blocks that allow the user to implement the DIO, event capture, event generation, and PWM I/O capabilities, all with 10 ns resolution, in the real-time model without coding.

This FPGA task mapping is only the first step toward Sim-On-Chip technology in which more general simulation tasks, for example a motor and its drive, are mapped to the FPGA core. In hardware-in-the-loop applications, this technology will permit to avoid the latency time of the PCI bus of standard PC by grouping model and I/O and simulation time step of 1 us are expected.

## III. ARTEMIS: Dealing with switched power networks in real time

The ARTEMIS software is a blockset from Opal-RT Technologies for the SimPowerSystems (SPS) blockset for Simulink. It permits real-time simulation of SPS schematics under Real-Time Workshop and RT-LAB software. ARTEMIS improves the real-time simulation capability of standard Simulink SPS schematics with the following characteristics:

- High precision discretisation methods in addition to the SPS trapezoidal rule of integration
- Equation parallelization of network containing distributed parameter lines or other decoupling devices.
- Cached precalculation of network equations for some or all switch position topologies (circuit modes).
- Interpolation for switching events occurring between time steps.

Precomputation of circuit modes due to switch position is critical to obtain real-time simulation performance from SimPowerSystems because it removes the mode equation calculation (i.e. finding the content of the A, B, C, D matrix) from the real-time

loop leaving only the iteration part (multiply-addition of A, B, C, D matrix with inputs and state vectors) in this loop.

Interpolation capability is an important feature in real-time simulation to keep acceptable accuracy despites the computational time constraint of real-time simulation. ARTEMIS interpolation algorithm [2] is especially designed to deal with this limitation by *avoiding* double interpolation scheme used in all other real-time simulation platforms.

Accuracy can also become an issue in real-time simulation because solvers are fixed-step type and non-iterative. Consider the series RLC circuit of Fig. 2 in which the switch is suddenly closed.

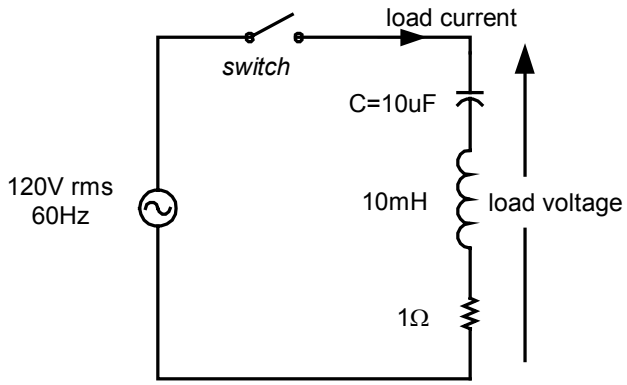



Fig. 2. Series RLC circuit

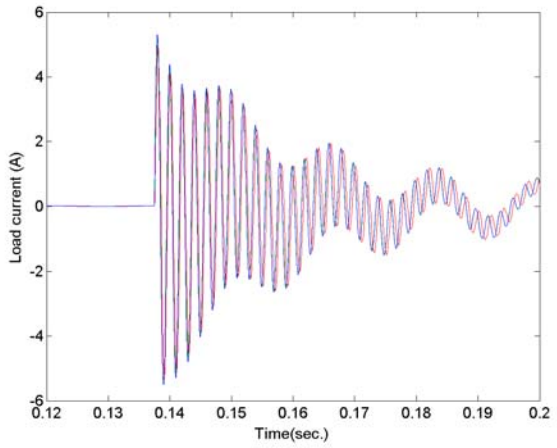



Fig. 3. Series RLC current response.

Fig. 3 and Fig. 4 show that **art5** discretization method of ARTEMIS matches closely the variable step solver of SPS while the Tustin method (fixed-step) of SPS has a phase shift (at 100 µs in both cases).

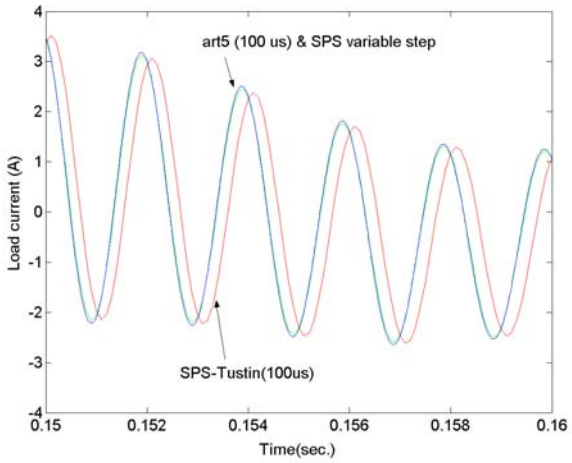



Fig. 4. Detail of series RLC current response.

## IV. RT-Events blockset: Dealing with high-frequency PWM inverters and DC-DC converters

The problem of electrical system simulation gets worst when simulating power converters like PWM motor inverters and DC-DC converters because of their high switching frequencies with regards to the simulation sampling frequency, i.e. the inverse of the time step. One of those problem concerns the accurate time sampling of IGBT gate signals. In AC motor drives for example, accurate motor flux integration is dependant upon the precise sampling of the IGBT gate signals by the simulator. This sampling must have sub-µs precision while typical real-time simulation time step are in the 10-50 µs range. There are solutions to this problem.

a) In fully numerical real-time simulation where controllers and plant are simulated, the IGBT gate signals generation must be made with equivalent sub-µs resolution despites the fixed-time simulation. This requires the use of RT-Events, a Simulink blockset designed for interpolation of in-step events in models like the sinus-triangular comparisons occurring in PWM generation.

b) In real-time HIL simulation where the simulated motor inverter is interacting with an external controller, the IGBT gate signals must be sampled by high frequency counter cards (like Opal-RT FPGA card) and the resulting time stamp incorporated into the simulation process by some interpolation technique.

In both cases, the IGBT bridge model must be able to use this interpolation information to compensate the simulation process.

Take for example the simple chopper drive of Fig. 5 where the load current should be linearly dependant upon the chopper duty-cycle. It happens that the simulation of this drive at 10 µs time step and a 10 kHz chopping frequency (PWM frequency to simulation sampling frequency ratio of 0.1) leads to gross inaccuracies when the simulation is uncompensated like in SimPowerSystems blockset with discrete simulation option (Fig. 6, curve *r*).

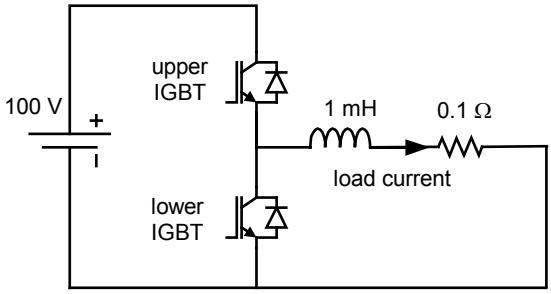



Fig. 5. Simple chopper

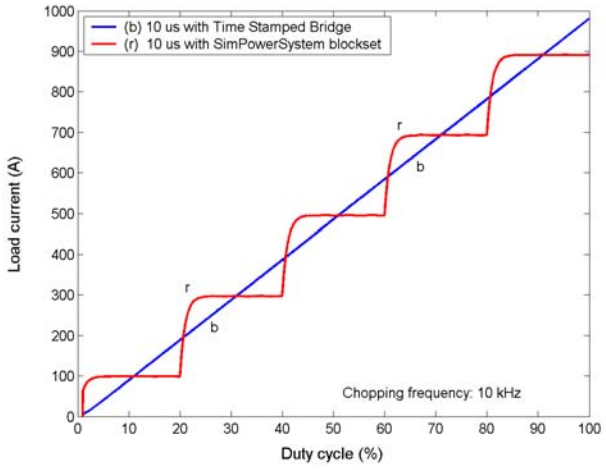



Fig. 6. Simple chopper load current as a function of duty cycle

In contrast, compensated fixed step simulation tools like the RT-Events blockset from Opal-RT Technologies lead to accurate simulation (Fig. 6,curve *b*). This works because RT-Events blocks propagate zero crossing information at fixed time step and the Time Stamped Bridge use this information to produce compensated output voltages.

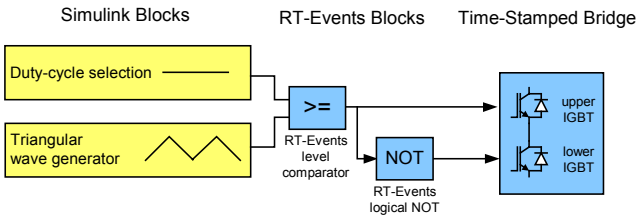



Fig. 7. Simulink blocks, RT-Events logical blocks and Time Stamped Bridge interconnection.

The Time Stamped Bridge models of the RT-Events blockset are an effective method to simulate power inverters. The technique is accurate on inverters working in continuous conduction mode. It must by noted that ARTEMIS could also deal with the same inverter with equivalent accuracy because of its interpolating capability. The Time Stamped Bridge is much faster though because it does not involve the state space formulation of network equations used in ARTEMIS and SimPowerSystems.

## V. Example of real time simulation of motor drive and other electric devices

This section will show some actual real time simulation of motor drives and electric systems. Those examples include basic drives like: PMSM drive with AC-side diode rectifier, train traction drive (3-level GTO inverter PMSM drive with 12-pulse thyristor rectifier), multi-level low harmonic inverter drive and induction motor drives.

Simulation of more complex power system like fuel cell hybrid electrical vehicle system and doubly-fed induction generator drive for wind turbines is also demonstrated.

Finally, real time simulation of complex distributed power electronic generation and distribution systems is done. Those include onboard military power system and a close replica of the Naval Combat Survivability DC Distribution Testbed with two synchronous generators.

All the cases show the importance of using interpolation techniques to obtain accurate simulation of high frequency inverters or DC-DC converters. In addition, when some line-commutated rectifier stage is present, the ARTEMIS plug-in is useful to gain real-time computational speed.

### A. Permanent magnet motor drive with AC-side diode rectifier

The circuit of Fig. 8 represents a permanent magnet motor drive fed by a 3-phase diode rectifier. The model runs under RT-LAB on a 2.8 GHz dual-Xeon PC at sample times of 10 µs for the motor inverter and 80 µs for the diode rectifier. The diode rectifier uses the ARTEMIS blockset to precompute all modes of the rectifier, thus removing SimPowerSystems mode computation from the real-time loop. A Time Stamped Bridges models the IGBT bridge is used to accurately compute the voltage-time application time to the motor model. This is important because if the model where to sample the IGBT gate signals at 10 µs without special care, important error would occur in the motor fluxes computation with the PWM carrier set at 9 kHz (~110 µs period, ~10 time the simulation time step).

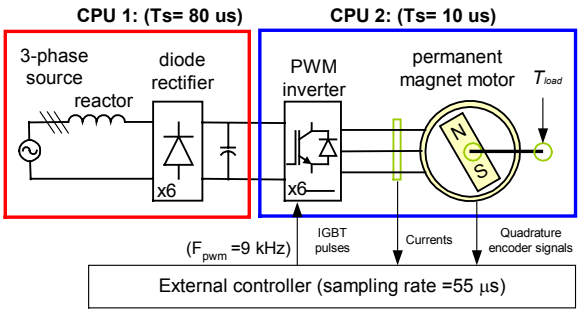



Fig. 8. PMSM drive with AC-side diode rectifier

Simulation results of the drive are shown in Fig. 9 and Fig. 10, using an internal Simulink controller. For this case, the speed command is varied in a square wave (10 Hz) fashion between 3000 and 600 rpm. Both figure show the Iq torque control effect that rises when the machine is required to accelerates and goes negative when the machine is commanded to decelerate. One can again notice that noise levels are much higher when the interpolation capability of Time Stamped Bridges is disabled.

A real-time simulator running this model has been successfully commissioned by Opal-RT for Mitsubishi Electric Co. of Japan in August 2004 [8]. The model is connected to a real external vector controller with a sampling rate of 55 µs. The external controller reads the motor currents and the quadrature encoder signals from the simulator and feeds the simulator with the 6 IGBT gate signals. The complete model run in this HIL mode at a sample time of 10 µs for the CPU simulating the inverter and 80 µs for the CPU running the AC-side of the model.

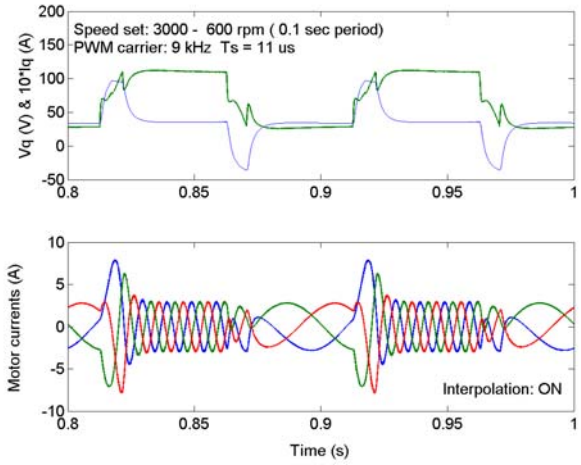



Fig. 9. Controller Vq Iq values and motor currents with Time Stamped Bridge interpolation enabled

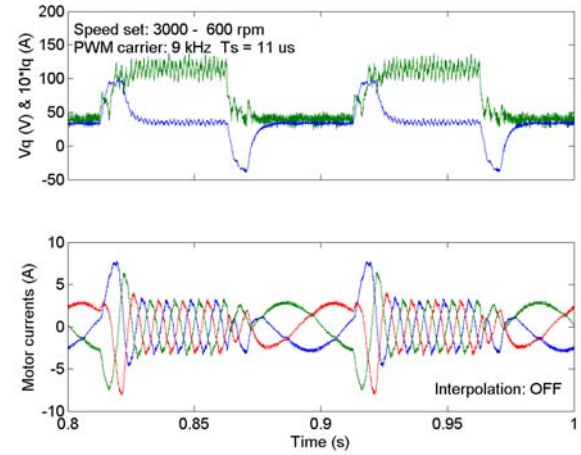



Fig. 10. Controller Vq Iq values and motor currents with Time Stamped Bridge interpolation disabled

| Table 1. PMSM drive with AC-side diode rectifier Real-Time Performance | |
|---|---|
| Target | 2.8 GHz Dual Xeon |
| RT-LAB version | 6.2.5 (QNX) |
| Ts (with I/O) | 10 µs |
| I/O description | 6 TS Digital Input,<br>3 Analog ouput,<br>2 TS Digital Output* |

* TS: Time Stamped, means high-frequency sampling and generation is made by the FGPA-board

## B. Fuel Cell Hybrid Electric Vehicle Drive

The circuit of Fig. 11 represents a fuel cell hybrid electrical vehicle drive system composed of a battery, a fuel cell, a DC-DC converter and motor drive [4][5].

In this system, the DC-DC converter controls the power sharing between the battery and the fuel cell. The use of Time Stamped Bridge is mandatory to obtain accurate simulation of the DC-DC converter because its chopping frequency (10 kHz) represent only 1/10 the period of the 10 µs model sample time. Errors on IGBT gate sampling can lead to uncontrollability in the real-time simulator. To show this point, the duty-cycle of the DC-DC converter has been scanned and the resulting inductance currents plotted in Fig. 12. The figure shows that the use of time-stamped bridges with a 10 µs time step (curve b) produces a smooth response that perfectly matches the results obtained with a very low time-step value of 1µs (r) with time stamps (i.e. interpolation). The response has an unacceptable staircase shape when the time stamps are deactivated, even at 1 µs (c & g). Fig. 12 also highlights the corner of the characteristic when the fuel cell diode turns off. This occurs when duty-cycles are greater than 0.52 (52%).

The results demonstrate that **the small-signal linearity is preserved with the time stamped bridge** while the uncompensated bridge causes the characteristic to have discontinuities. Without time stamps, it is clear that the circuit would be hard to control, if not at all.

The model runs under RT-LAB on a 2.8 GHz dual-Xeon PC at sample times of 10 µs. With 6 Time Stamped digital inputs and 5 analog outputs, the sample time rises to 17 µs.

Table 2. Fuel Cell Hybrid Electric Vehicle Drive Real-Time Performance

| | |
|---|---|
| Target | 2.8 GHz Dual Xeon |
| RT-LAB version | 6.2.3 (QNX) |
| Ts min without overrun (no I/O) | 9 µs |
| Ts min without overrun (with I/O) | 17 µs |
| I/O description | FPGA: 6 DIN, 5AO |

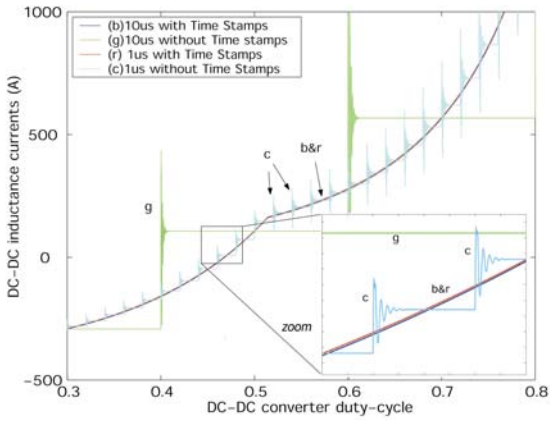



Fig. 12. DC-DC converter inductance current characteristic vs. interpolation usage

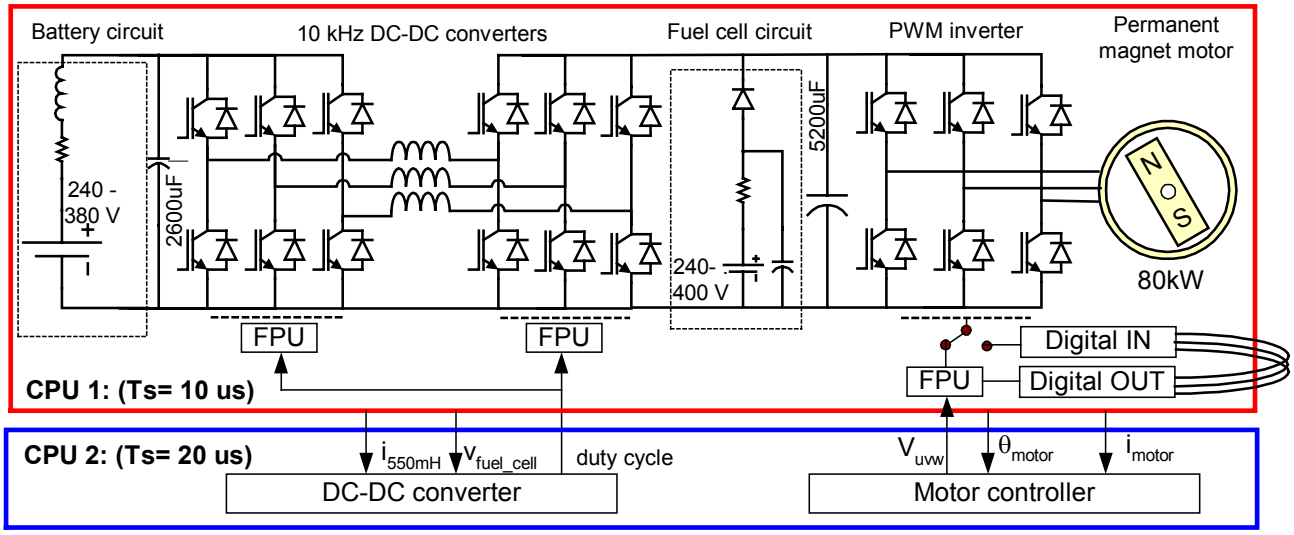



Fig. 11. Fuel cell hybrid electric vehicle drive circuit with numerical controllers and task separation (below)

### C. Doubly-fed induction generator for wind turbine applications

Fig. 13 describes a wind-turbine doubly fed induction generator connected to a grid circuit[3]. The inductive grid, transformers and induction machine are modeled in SimPowerSystems. The two PWM inverters are modeled with Time Stamped Bridges. The 7.5 kW doubly fed induction machine with back-to-back PWM inverters is based on reference [1] and used the exact same parameters except the compensator gains and PWM carrier frequency. In all tests, the PWM carrier frequency is set to 2 kHz and the simulation step size is 50µs. A more elaborate description of the set-up used for the real-time simulation of this model can be found in reference[3].

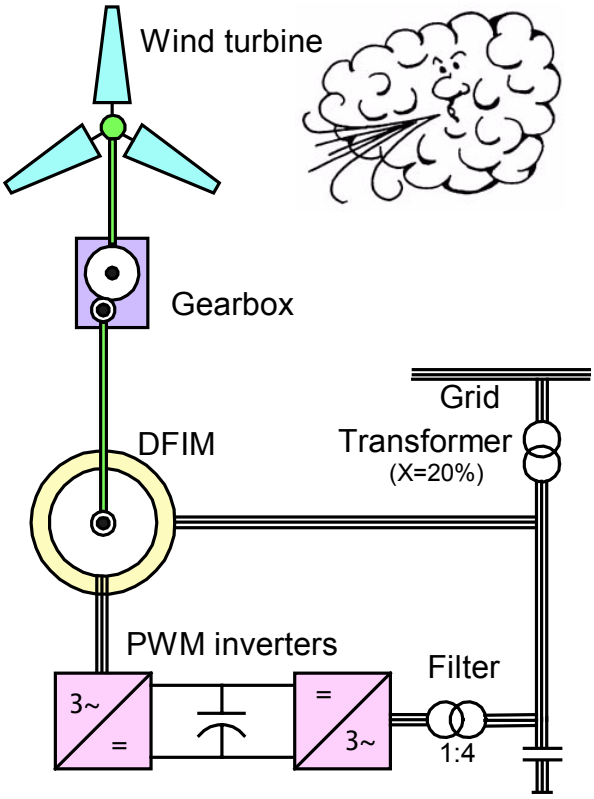



Fig. 13. Doubly-fed induction machine wind generator circuit

A test is made to show the operation of the wind generator when the rotor speed goes from hypersynchronous to subsynchronous operation. The capability of the DFIM with back-to-back PWM inverters to work easily across the null slip point is an interesting aspect of this topology. The rotor speed scan has been made in a time lapse of 2 sec. Fig. 14 shows the rotor currents during the rotor speed change. While changing the rotor speed, the power controllers try to keep the stator active and reactive powers at their commanded values with some success (Fig. 15).

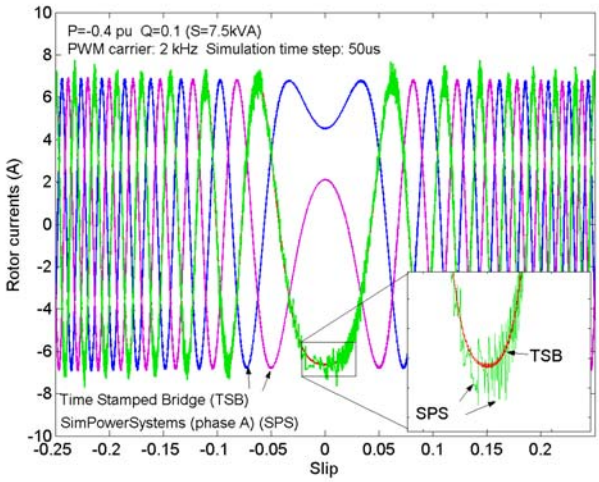



Fig. 14. Rotor currents for operation across synchronous speed

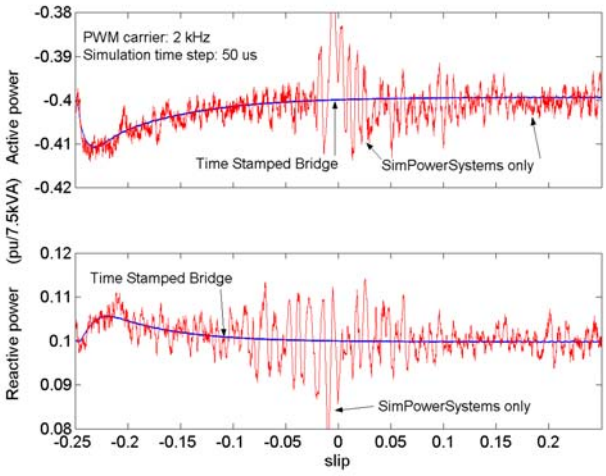



Fig. 15. Powers at stator during slip scan

On Fig. 14, the rotor current for phase A is superposed with the case where the rotor-side inverter is modeled with Simulink SimPowerSystems blockset working in discrete mode. A section of the simulation is zoomed and shows that SimPowerSystems simulation for the rotor-side inverter is the source of inaccuracies. By contrast, usage of Time Stamped Bridges results in smoother rotor currents more compatible with the 2 kHz carrier frequency of the inverter. Inaccuracies are also visible at the stator power level when the simulation is not compensated with Time Stamped Bridges.

## D. Train Traction Drive

The train traction drive described in Fig. 16 is composed of a grid-connected 12-pulse thyristor rectifier connected to a 3-level GTO inverter feeding a 1 MW permanent magnet motor.

The 3-level GTO inverter is modeled with Time Stamped Bridge and ARTEMIS was used to achieve hard real-time simulation of the AC-side rectifier. Furthermore, a special transformer model was designed to artificially decouple the two secondary windings of the transformer so full precomputation of the two 6-pulse thyristor modes could be made by ARTEMIS. If this is not done then the algorithm would have to precompute 2^12 = 4096 different system equations for the AC-side only.

The principle used to introduce the decoupling at the secondary windings is to model the secondary leakage inductance by a short transmission line having the same line inductance. The approximation has then the effect of introducing some line capacitances that are not really present in the circuit. As long as the sample time is small, the spurious capacitances are also small and the error is minimal.

The model takes advantage of the fact that the voltage of the DC-link capacitors do dot change much during a single time step and therefore introducing delays in voltage output to CPU #2 and bridge current inputs from the same CPU cause minimal errors.

Fig. 16. Train traction drive model with task separation (below)

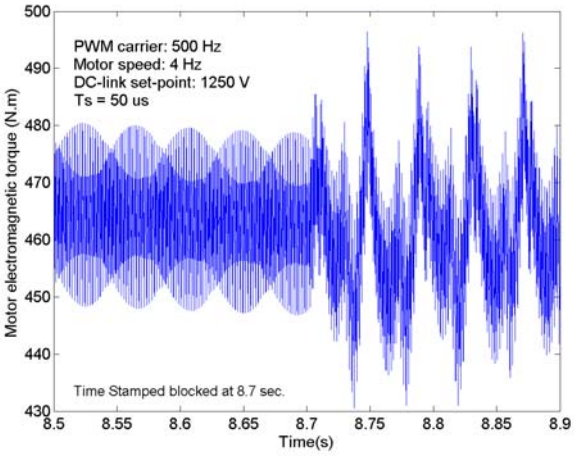
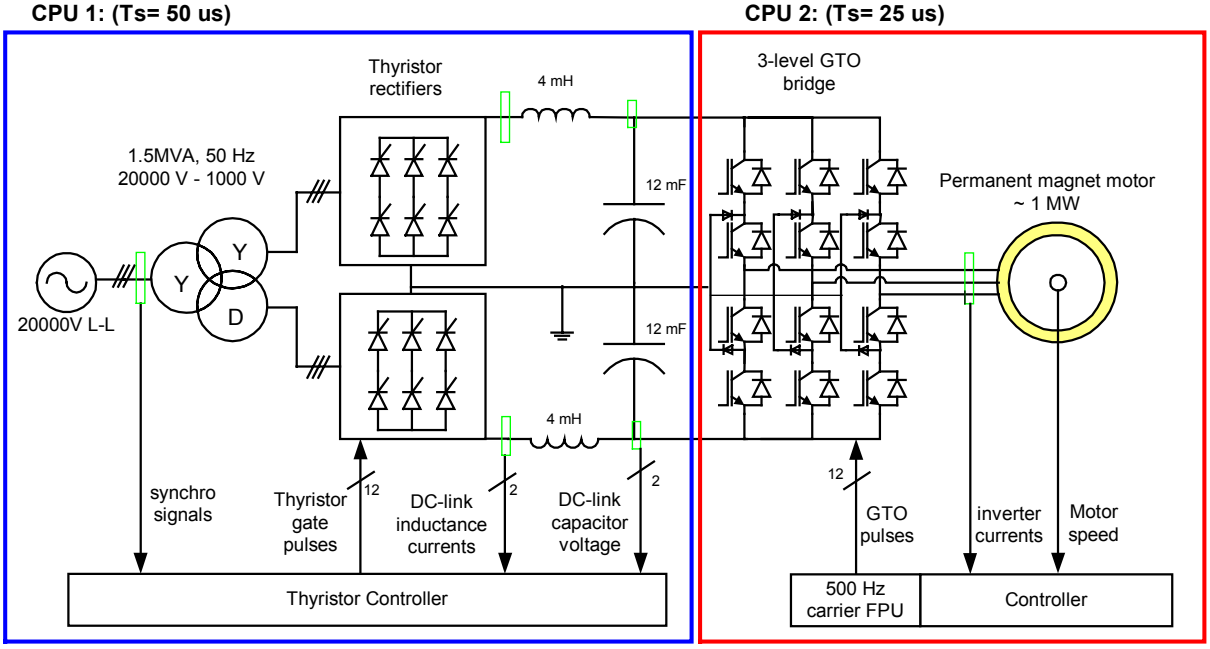



Fig. 17. Simulated electromagnetic torque: Effect of disabling interpolation

The effect of using RT-Events generated PWM pulse in this simulation are best viewed in the electromagnetic torque of the PMSM motor. Fig. 17 shows that the simulated electromagnetic torque of the machine becomes noisy when the interpolation is disabled after 8.7 sec. of simulation.

This complete drive with numerical (Simulink) controllers runs at sample time of 19 µs with no I/O present on a 2.4 GHz Dual Xeon PC running RT-LAB 7.0b4 with RedHawk Linux operating system.



## E. Military vehicle onboard power system

The circuit of Fig. 18 represents a military vehicle onboard power system. The main power source is a diesel motor driving an alternator which output is rectified to produce a 600VDC bus voltage used primarily for vehicle traction. The 600V voltage is converted by a DC-DC converter to 26VDC for the hotel loads. In the case presented, this load consists of a DC motor and an AC inverter with its load.

The diode rectifier uses the ARTEMIS blockset to precompute all modes of the rectifier, thus removing SimPowerSystems mode computation from the real-time loop. The traction motor, DC-motor chopper and AC inverter use Time Stamped Bridge which use special interpolation techniques to accurately compute the voltage-time application time to the motors and load. This is important because if the model where to sample the IGBT gate signals at 30 µs without special care, important error would occur in the motor fluxes computation with the kHz-range PWM inverters.

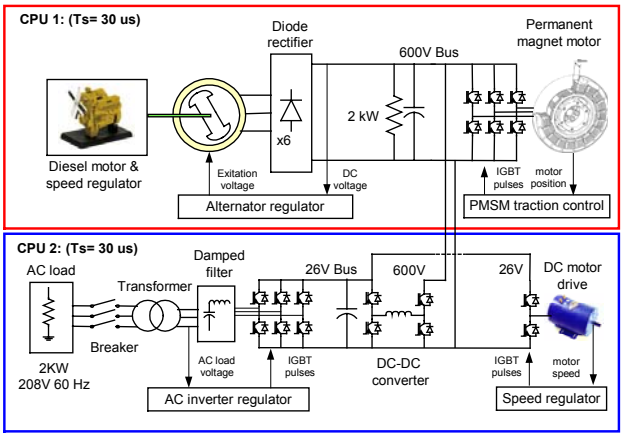



Fig. 18. Schematic with task separation of military vehicle onboard power system

Fig. 19 and Fig. 20 show the importance of using interpolation when simulating the IGBT inverter. The DC-motor drive has a chopping frequency of 2.5 kHz. For the selected simulation time step of 30 µs, the DC-motor simulation accuracy is unacceptable when SimPowerSystems bridge model (non-interpolating method) are used (Fig. 20). When Time Stamped Bridges (Fig. 19) are used, accuracy is much better. The latter case is precise enough to show the small speed variation caused by the low frequency 26 VDC bus voltage variations.

The model runs under RT-LAB on a 2.8 GHz dual-Xeon PC at sample times of 30 µs for the motor inverter. This time step includes Hardware-in-the-Loop simulation of the IGBT gate signal of the AC-inverter and breaker controls that are sent from the Simulink controller through the Opal FPGA I/O card outputs then immediately read back as input to the model (set-up used only for testing purposes).

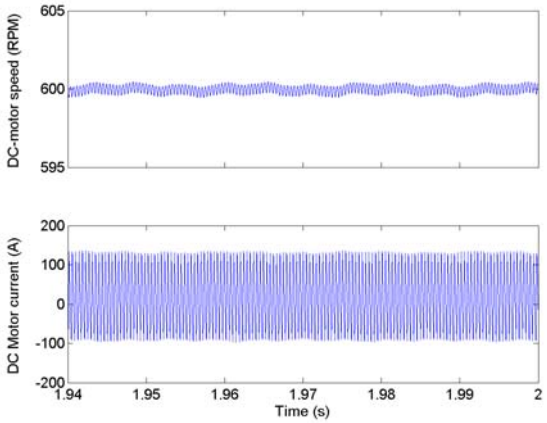



Fig. 19. Simulation accuracy of the DC-motor currents and speed. With Time Stamped Bridges

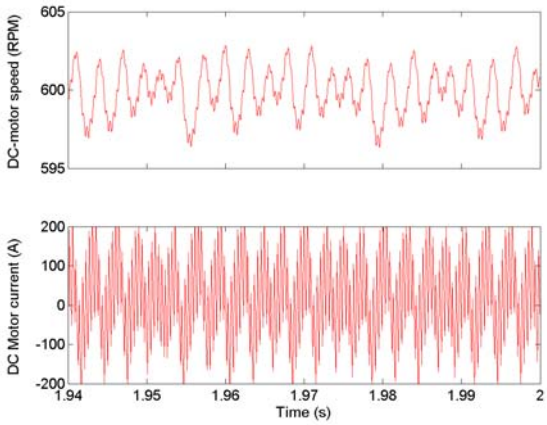



Fig. 20. Simulation accuracy of the DC-motor currents and speed. Without Time Stamped Bridges

| Table 3. Military vehicle onboard power system Real-time Performance | |
|---|---|
| Target | 2.4 GHz Dual Xeon |
| RT-LAB version | 7.0b4 RedHawk Linux |
| Minimum sample time without overrun (no I/O) | 21 µs |

## F. Naval Combat Survivability testbed

Next-generation all-electric warships will be equipped with highly complex distributed energy generation and distribution systems that must be capable of operating under very stringent conditions.

These systems will include several power electronic systems, interconnected by AC and DC busses to feed a variety of complex loads and controls. The design, test, commissioning, operation and maintenance of such systems will be a real challenge due to the complexity of the total interconnected system. In particular, the stability assessment of such systems will be very challenging.

The Naval Combat Survivability testbed are reduced-scale power systems developed in collaboration with the U.S. Navy to study various aspects of all-electric war ships like multi-converters interactions and overall stability.

Lately, some attempts have been made to complement the testbeds with a real-time simulator implementing additional subsystems[7]. In this section, we try to demonstrate the capability of the RT-LAB simulator to simulate such complex system.

The simulated system, described in Fig. 21 with the task separation on 2 CPUs, is composed of the complete NCS Generation testbed along with two synchronous machine generators. In the system, each generator feed one of the DC busses. From each bus, Ship Service Converter Module (SSCM) feed each load in a redundant way so that if power fails on one bus, the load can be fed from the other bus. There are 3 different loads connected to the buses through the SSCM: an induction machine, a power inverter and a Constant Power Load.

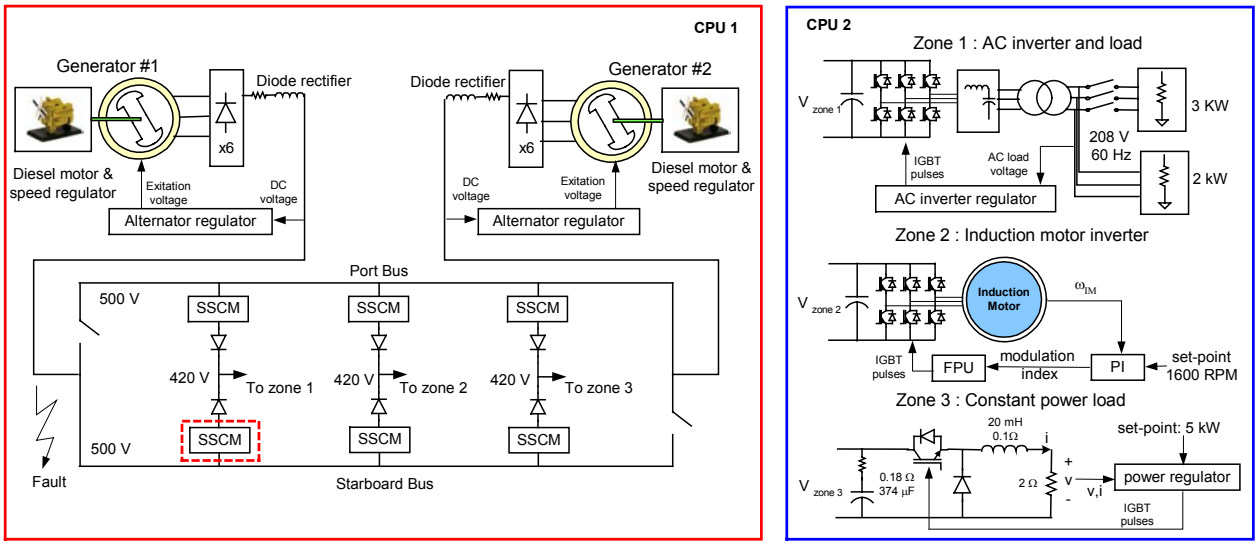
Controllers on the simulated system are not the same as in the real testbed. For example, the SSCM module have simple PI voltage output feedback. This is just a question of simplification except for one aspect: the PWM carrier frequency that is set to 2 kHz or less for all converters, i.e. 10% of the simulation sampling rate (Ts=50 µs). This limitation comes from the Time Stamped Bridge themselves which becomes less accurate when the PWM frequency to simulation sampling frequency ratio becomes greater than 0.1-0.2. With simulation at fixed time step using standard software like SimPowerSystems of Simulink, the same loss of precision occurs at ratio nearer 0.01-0.001 so the Time Stamped Bridge offers a 10 to 100-time improvement on standard non-iterative fixed step simulation.

A simulation case was carried out on the alternator augmented NCS Distribution model (Fig. 21) in which a ground fault is made at the Starboard bus. As can be expected, the fault affects all bus voltages. The validity of the real-time simulation waveforms at 50 µs is confirmed by simulating the same system at a time step 10 times lower.

The simulation results are shown in Fig. 22 and Fig. 24, showing the bus voltages. Fig. 23 and Fig. 25, show the inverter modulation index and output voltage, the induction motor speed and torque and the power of the Constant Power Load. On these figures, one can observe that the responses are somewhat similar.

This complete system runs at sample time of 37 µs with no I/O present on a 2.4 GHz Dual Xeon PC running RT-LAB 7.0b4 with RedHawk Linux operating system.

Fig. 21. NCS Distribution testbed with alternators model (below)



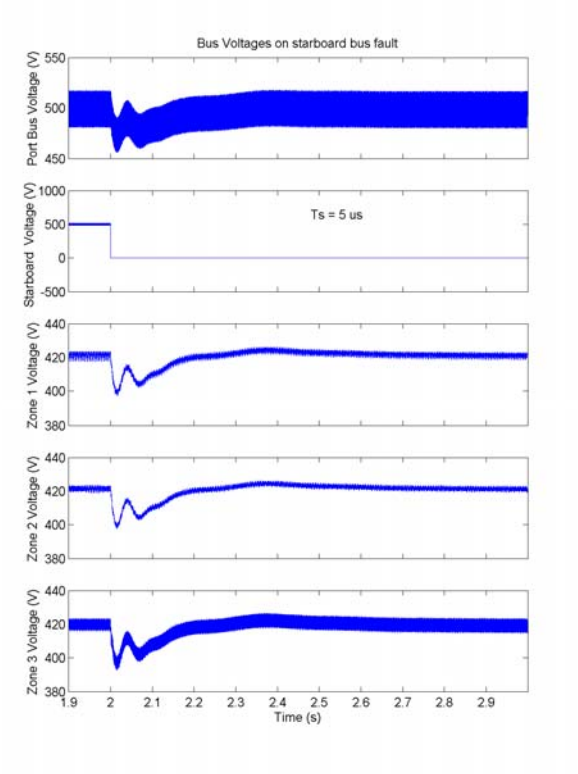



Fig. 22. Bus voltages on starboard bus fault (Ts= 5 µs)

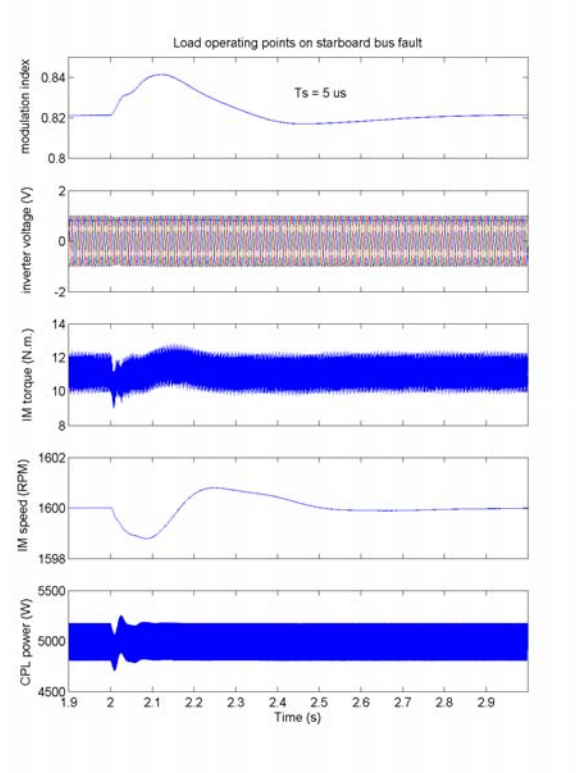



Fig. 23. Load operating points on starboard bus fault (Ts= 5 µs)

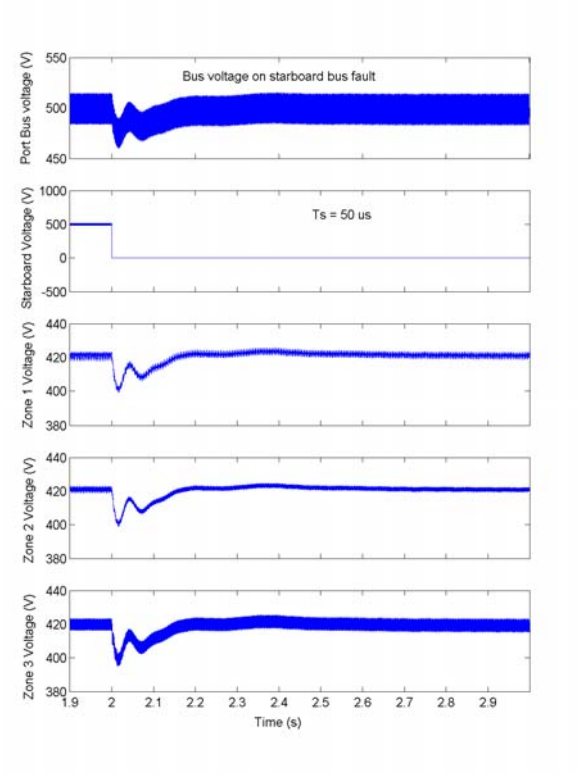



Fig. 24. Bus voltages on starboard bus fault (Ts= 50 µs)

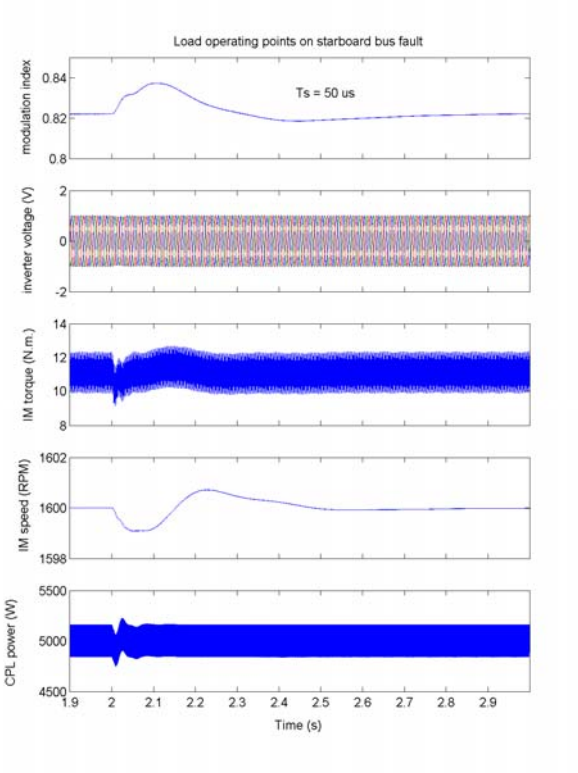



Fig. 25. Load operating points on starboard bus fault (Ts= 50 µs)

### G. Nine-level inverter with 13-winding three-phase transformer

The multi-level inverter shown in Fig. 26 is a high-power ultra-low harmonic generating inverter drive. By feeding the DC-stage from winding with different phases, the injected harmonics are minimized at the primary. Nine-level inverter also provides low harmonics at the load. Time Stamped Bridges are used to model the inverter part while a special decoupling transformer in conjunction with ARTEMIS permits full mode precomputation of this model and achieve real-time simulation under 80 µs time step on a dual Xeon 2.4 GHz computer.

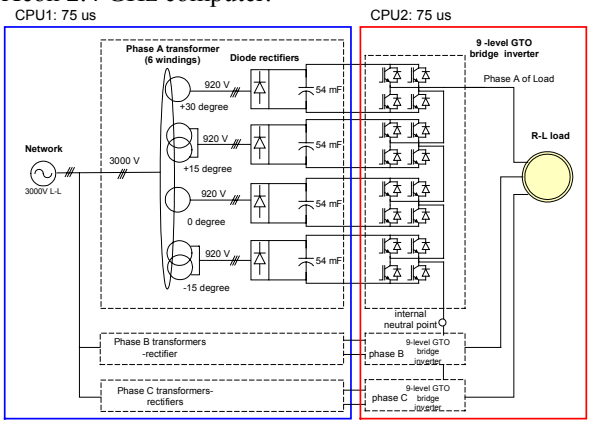



Fig. 26. Nine-level inverter with feeding transformer

### H. Parallel bridge induction motor drive

A critical aspect of the parallel bridge induction motor drive of Fig. 27 is the individual firing delay between parallel IGBT, which can cause huge current spikes in the interphase transformer[6]. Advanced Time Stamped Bridge model permits to vary individual IGBT characteristics and study this effect in real-time.

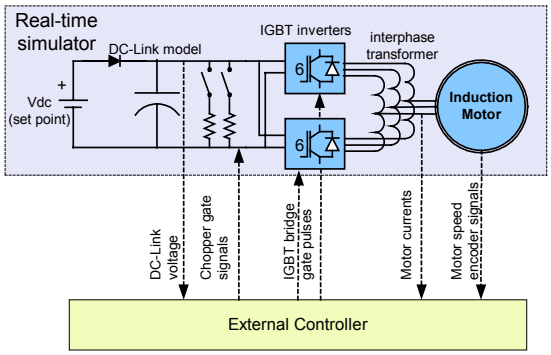



Fig. 27. Parallel inverter induction motor drive

## VI. Conclusion

This paper has presented the RT-LAB simulator and demonstrated its capability to make real-time simulation of motor drives and complex power electronic generation and distribution systems.

The paper has also explained the special simulation tools developed by Opal-RT to enable real-time simulation like RT-Events and ARTEMIS. All the studied case had some high frequency power converter built-in and it has been demonstrated that the use of interpolation technique was mandatory to obtain accurate results.

The RT-Events blockset and especially the Time-Stamped Bridges models were demonstrated to provide for the necessary accuracy to make the real-time simulation of power systems with 2-10 kHz PWM inverters in the 10 to 50 µs time step range.

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