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Real-Time Simulation of a Complete PMSM Drive at 10 µs Time Step

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Abstract – This paper presents a description and results of the fastest-ever-reported, PC-based real-time (RT) simulator of an AC drive. The RT simulator is used to simulate a complete PMSM drive circuit in a Hardware-In-The-Loop (HIL) application. This consists of a PMSM fed by a 3-phase IGBT inverter, a DC link capacitor and a 3-phase diode bridge. This drive model runs on RT-LAB electric drive simulator and is connected to an external controller by analog and digital inputs and outputs for closed loop operation.

The main innovation in this work is that the real-time simulation cycle is as low as 10 µs, which constitutes –to our knowledge- the shortest RT simulation time step ever reported for electric drives with this level of details in modeling the drive circuit.

Keywords: Real-time, simulation, Hardware-in-the-loop, Simulink, RT-LAB, motor drive, PMSM, HIL.

1. Introduction

Due to the increasing complexity and costs of projects, and the growing pressure to reduce the time-to-market, testing and validation of complex systems has become more and more important in the design process.

With the great advancement in processor and software technology and their cost decrease, it has become possible to use gradual and complete approach in system design, integration and testing; this approach, which has been traditionally reserved to very large and complex projects (power systems, aeronautics, etc.) is the real-time (RT) simulation.

For AC motor drives, RT simulation is used to connect a part of the system or its prototype to a RT digital model of the remaining part of the system, in what it is commonly called Hardware-in-the-Loop (HIL) application.

The most critical criterion in conducting a RT digital simulation is how to attain acceptable model accuracy with an achievable simulation time-step. This is especially a challenging task for the simulation of switching power electronics and motor drives. These highly non-linear systems need very tiny time-steps to reach acceptable accuracy.

Great improvement of processing power and resources were obtained during the last two decades – along with a fast decrease of their cost – mainly due to the mass market of personal computers. But even with today's GHz-speed processors, practical time step achievable by high-end HIL simulators like RT-LAB [(1)], dSPACE [(2)], and RTDS [(3)] rarely goes beneath 25 µs for different reasons related to Inputs/Outputs (I/O) and communication latencies, but also to the solving methods.

However, if this simulation time-step limitation may be acceptable for power systems, that can be accurately simulated with time step of 50 to 100 µs (10 to 20 kHz), a minimum time step as low as 25 µs may be not acceptable for some demanding applications, like switching motor drives simulation. The increasing switching frequency for small and medium power drives is pushing the simulation sampling frequency above 40 kHz.

This paper will describe the implementation of a RT simulation of a Permanent Magnet Synchronous Motor (PMSM) drive on RT-LAB Electrical Simulator with a simulation time-step of 10 µs (sampling frequency of 100 kHz), which to our knowledge constitutes the fastest ever reported HIL digital simulation of motor drives, using commercial hardware and software.

2. PMSM Drive

The PMSM drive used consists of a 3-phase motor, fed by an IGBT inverter connected to a capacitive DC link; this latter is charged by a 6-diode rectifying bridge connected to the 3-phase AC main, as is illustrated in figure 1. Typical parameters of the drive are given in Table 1.

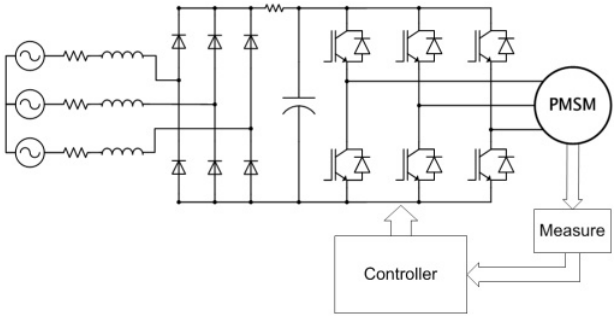

Fig. 1. PMSM Drive Circuit

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Table 1. IPM Motor Parameters

Points	Value	Unit
Motor rated power	7500	W
Motor rated speed	1800	r/min
Motor rated torque	39.79	Nm
PWM frequency	2.25, 4.50, 9.00	kHz
Dead time	4.2, , 9.8, 12.6	µs

3. Setup Description

3.1 Objective

The objective of the project is to test and optimize the controller including the firing module; testing and validation is to be conducted by the means of a real-time digital simulator that simulates the drive circuit, including the AC-DC diode converter, the 6-IGBT inverter and the AC motor.

3.2 Setup

The complete setup of this HIL application is illustrated on Fig. 2.

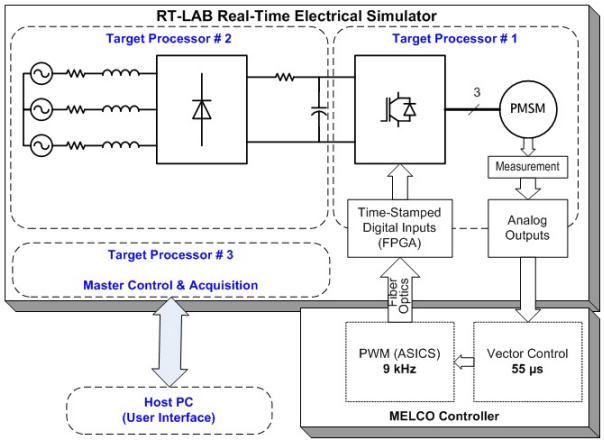


Fig. 2. HIL Setup of the PMSM drive

The setup consists of two main parts: the controller and the drive circuit.

The controller includes a control module and the PWM generator board. The vector control runs at 55 µs and the PWM carrier frequency can be varied up to 9 kHz.

The drive circuit is implemented in Simulink and uses the RT-Events toolbox [4]; it is simulated in RT on RT-LAB electrical simulator; the drive is simulated by two target processors, Pentium 4, 2.8 GHz each: one for the AC-DC part, and one for the DC-AC part including the motor; the separation is made at the capacitor level, which is large enough so that the delay introduced by the inter-processor communication affects very little the DC voltage that stays nearly constant during one simulation step. A third Pentium processor is used for master control of the simulator and for data acquisition sent to a remote host, by a 100 Mb Ethernet link.

These two parts, the controller (external) and the circuit (simulated), operating in closed loop, use two means of communication: analog outputs, to send measured currents and speed signals from the RT simulator to the controller; and fiber optics to send the 6 PWM signals from the PWM board to IGBT inverter model.

The Simulink model is illustrated on fig. 3. Note that the controller and PWM generation are used in fully-digital simulation mode. The PWM firing uses blocks from the RT-Events toolbox for precise modeling of the switching signals; this is done through interpolation/compensation scheme embedded in RT-Events.

In the normal mode of operation which is the HIL mode, the gate switching signals, instead being locally generated (inside the simulator) come from the external controller under test. They are precisely captured by high resolution FPGA-based digital inputs as explained in the following section.

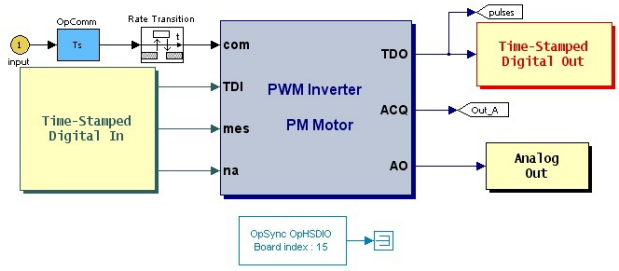


Fig. 3 (a). Top Level Simulink Model of the HIL setup

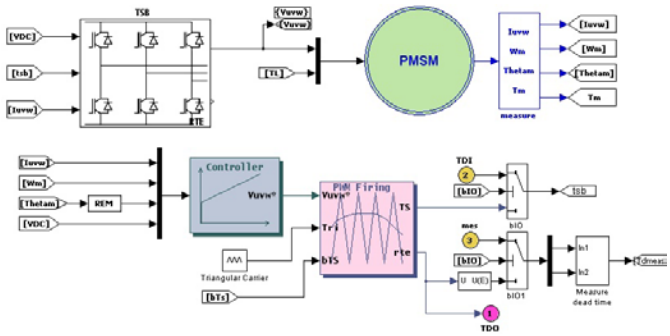


Fig. 3 (b). Simulink Model of the AC motor drive

3.3 Time-Stamping of Gate Signals

The PWM signals with a switching frequency of several kHz cannot be sampled by the simulator at the simulation frequency; this is because achieving the necessary resolution for gate signals would need a sampling time that is lower than 1 µs, and this is unreachable with the current state of technology. Therefore, in order to precisely capture the gate signals in the simulator, a high resolution timer board is used. This is an OP5110 [5], Xilinx FPGA board, with a clock of 100 MHz, capturing the PWM signals with a resolution of 10 ns.

By capturing the PWM signals with the FPGA board, the times of rising and falling transitions are recorded; then this timing information is forwarded to the IGBT's. In order to make use of transition times, special IGBT inverter model is necessary; this is done by using a time-stamped inverter model from RT-Events [4] that implements interpolation for fixed-step simulation of voltage source inverters and PWM generation units.

Due to the use of FPGA board to capture the PWM gate signals and of time-stamped, interpolated inverter model, it is possible to get rid of the jitter problem, encountered when simulating switching converters at a large fixed time step, along with all the non-characteristic harmonics and other anomalies associated with the jitter problem. In addition, *it is possible to take into account the effect of the dead time* even if it is much smaller than the real-time simulation step, as is shown by the experimental results.

4. Results

Several experimentations were conducted; some of the results are presented hereafter.

4.1 Performance Results

The minimum simulation step that can be achieved without overruns with the HIL setup shown in fig. 2 was 9 µs; this includes, in addition to the circuit model, 6 PWM inputs and 6 analog outputs.

4.2 Comparison of RT simulation and off-line simulation

In this experiment, the HIL simulation is compared to the conventional off-line simulation, where the complete drive model, including both the circuit and the controller is simulated in the Simulink environment. The inverter is modeled with the SimPowerSystem Blockset and the firing generation does not use the RT-Events toolbox but native discrete blocks of Simulink.

Fig.4 (a) shows the result of a conventional off-line simulation with a fixed time step of 10 µs. Because of this large fixed time step, the motor current waveforms and the torque present non-physical spikes that produce non-characteristic harmonics caused by the jitter on the PWM signals.

This jitter and the oscillation it causes on the current and voltage waveforms can be minimized, either by reducing the simulation step to very low values, as in Fig.4 (b) and (c), values that are not today achievable in real-time, or, if real-time operation is needed as in the present application, by using interpolation technique for both the switches and the firing and in case of HIL operation with external controller, very precise and fast time-stamped digital input boards are needed; this real-time solution was demonstrated by the RT-Events toolbox (interpolation of power electronics and discrete signals) and the FPGA board with 10 ns resolution, used to capture the PWM gate signals; the result is shown in Fig 4 (d).

Speed of simulation: the off-line simulation with 0.25 µs step size was 266 times slower than real-time; the platform used was a PC with dual Xeon CPUs of 3.06 GHz each.

4.3 Effect of PWM carrier frequency

The carrier frequency was set respectively to 2.25, 4.5, and 9.0 kHz; the effect of this frequency on the oscillation of the current waveforms was verified, as shown in Fig.5. Experiment parameters are: Motor speed = 1,800 r/min, Motor torque = 16.0 Nm, Dead Time = 4.2 µs.

The comparison of currents of both the HIL simulator and actual physical system shows they are very similar for all carrier frequencies.

4.4 Effect of dead-time

Moreover, the well-known current distortion caused by an increased dead-time was verified and validated; the current waveforms obtained with a dead time of 4.2, 9.8 and 12.6 µs respectively are shown in Fig.6. Experiment parameters are: Motor speed = 1,800 r/min, Motor torque = 16.0 Nm, Carrier Frequency=9.00 kHz.

That the real-time HIL simulator can model and precisely simulate the dead-time is particularly needed to test new algorithms for the compensation of the dead-time and the minimization of its distortional effect.

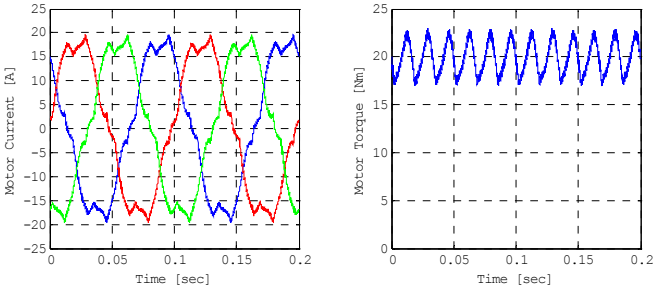


Fig. 4 (a). Off-line simulation with time step size 10.00 µs

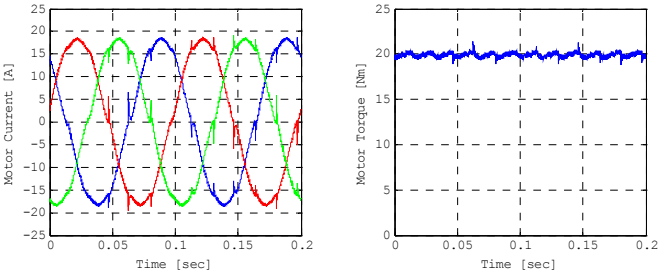


Fig.4 (b). Off-line simulation with time step size 1.00 µs

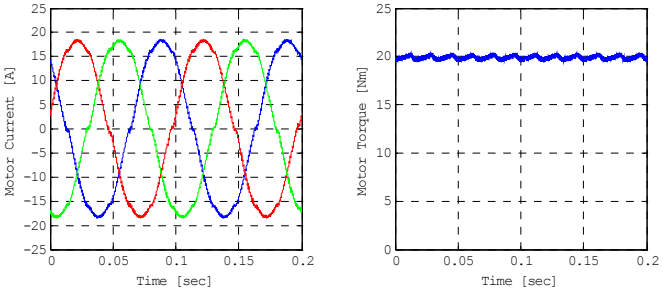


Fig.4 (c). Off-line simulation with time step size 0.25 µs

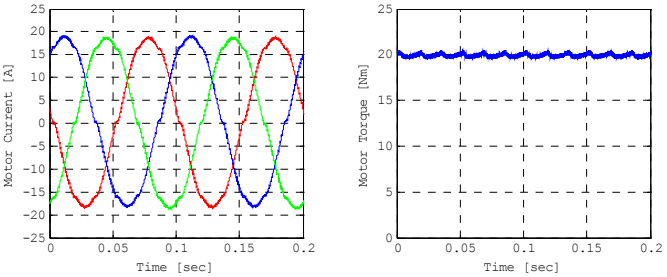


Fig.4 (d). Real-time simulation with time step size 10 µs

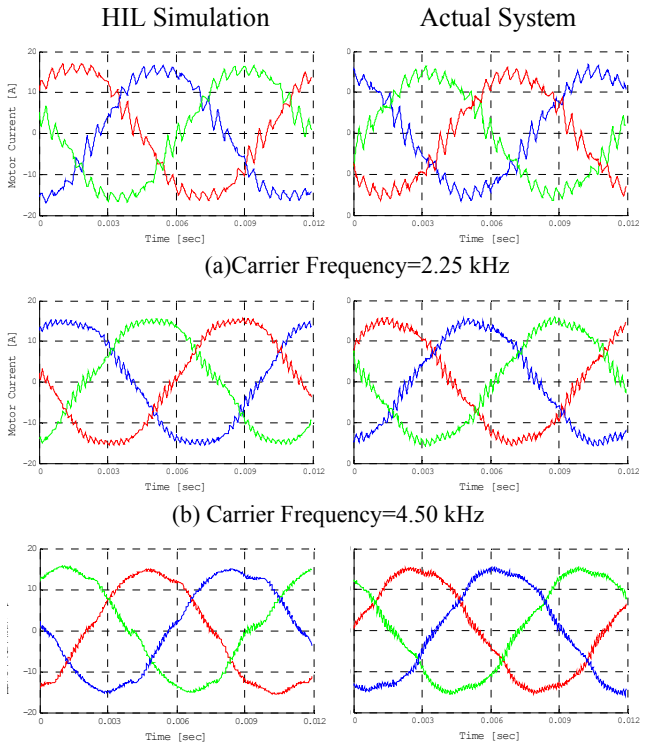
4.5 Speed step response

Another example of the real-time simulation using RT-LAB electrical simulator is shown in Fig.7. It shows the result of the speed step response, the motor speed reference changes from 0 to 1000 r/min, then back to 0. The RT HIL simulation result is compared to actual speed step response, demonstrating how close the waveforms for currents, torque and speed in both cases are.

5. Conclusions

This paper presented the description and results of the real-time simulation of a complete PMSM drive circuit in a Hardware-In-The-Loop (HIL) application. What is unique in this work is that it constitutes, to our knowledge, the fastest ever-reported real-time simulation of an AC motor drive, with precise simulation of power electronic switching and with such a high PWM frequency of 10 kHz. The work shows how it is possible to simulate this high frequency switching power circuit at time step of 10 µs, much higher than the step size needed if the techniques implemented in the RT-LAB electrical simulator are not used; these techniques includes interpolation, time-stamping of gate signals, parallel processing and the use of fast FPGA-based I/O's.

It is in the intention of the authors to pursue decreasing the time step to test higher switching frequencies by the use of more powerful – yet always commercial – hardware and by other optimization means, currently under development.

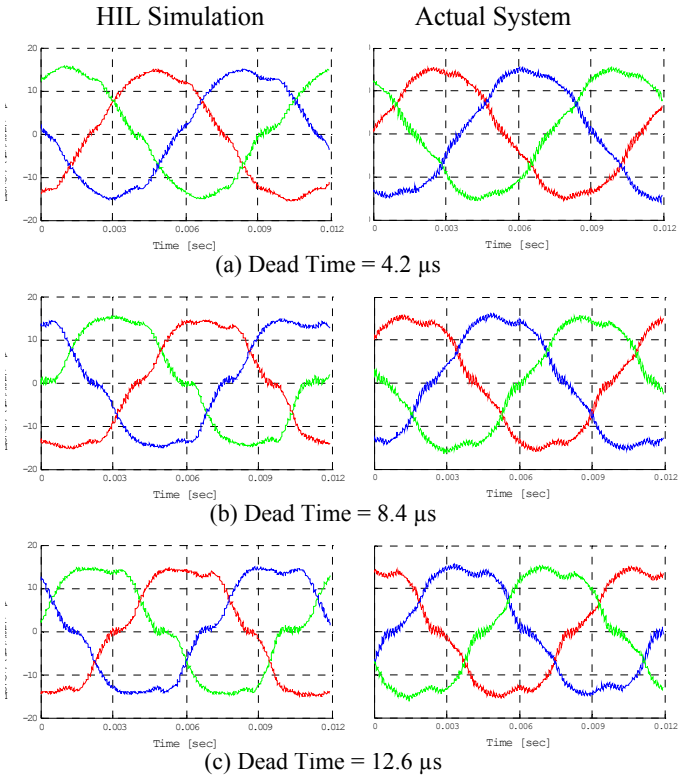


(a)Carrier Frequency=2.25 kHz

(b) Carrier Frequency=4.50 kHz

(c) Carrier Frequency=9.00 kHz

Fig.5. Effect of PWM carrier frequency



(a) Dead Time = 4.2 µs

(b) Dead Time = 8.4 µs

(c) Dead Time = 12.6 µs

Fig.6. Effect of dead time

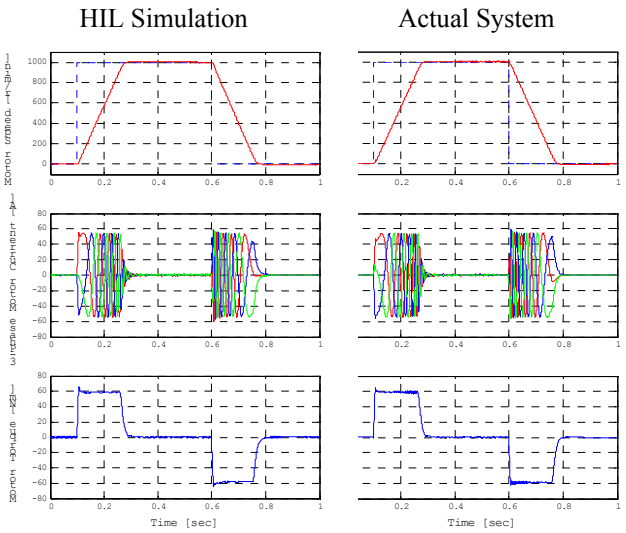


Fig.7. Speed step response

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