A 3-Level Neutral-Clamped Inverter Model with Natural Switching Mode Support for the Real-Time Simulation of Variable Speed Drives

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***Abstract*- This paper presents a simulation model of a 3-level Neutral-Point Clamped IGBT inverter bridge suitable for real-time simulation testing of Variable Speed drives. The model is based on the switching-function approach, but also implements natural switching modes like Hi-impedance and rectification when no pulses are applied to the inverter. The model can manage a Pulse Width Modulation (PWM) with a sample period to PWM period ratio up to 0.1 while remaining accurate through the use of interpolation methods. The switching-function approach produces exceptional computational speed gain when compared to piecewise time-segment linear algorithms such as MATLAB/Simulink using the SimPowerSystems or PLECS libraries and can allow these simulations to be conducted in real-time at sample times of 40µs. Real-time simulation results including Hardware-In-the-Loop (HIL) applied to electrical power conversion systems for Marine applications are presented in the paper.**

I. INTRODUCTION

The integration, test and verification of modern power systems always represent a serious challenge. Whereas it is not conceivable to proceed to a full scale validation test of the system, real time simulation with a physical controller in the loop allows an exhaustive validation of the control system interfaced with real responses of the physical plant.

Modern design approaches mitigate the risks through the extensive use of technologies like Hardware-In-the-Loop (HIL) simulation and the model-based design approach. In HIL simulation [1], a plant controller is tested against a real-time simulated model of the plant. HIL simulation technologies enable more gradual integration, while diminishing the risk and costs of such projects. Also, more elaborate test coverage can be conducted than is possible using analog prototypes because of the safe operational limits of real devices and plants.

Model-based design is an approach that puts the system model at the center of the design process [2]. With this approach, the specification, controller prototype design, coding and integration tests are based on a set of reference models. At the design stage, the approach makes an extensive use of automated code generation methods. At the integration stage, this approach makes extensive use of HIL simulators, with a number of objectives that are directly related to the specifications of the overall system.

The real-time simulation of complex drive systems is difficult for several reasons. The main difficulty resides in the large number of switches that a system contains. Typical power system solvers based on binary modeling of switches, such as SimPowerSystems, need to recalculate equations each time a switch conduction state changes and this causes important calculation time spikes that are not allow in hard real-time application such as HIL.

Switching function-based inverter models can alleviate these problems because they do not include the switch in the main system equations. Instead, they mimic switch actions by 'routing' voltage and currents across the components to which they are connected. This type of model usually assumes the condition of constant conduction of the load. When the condition is not fulfilled, this kind of model will not work [3]. This is the case when, for example, all IGBT gate pulses are stopped and load current drops to zero.

In [4], a switching-function based three-level neutral-clamped inverter was designed to support hi-impedance and rectifying modes. The model was cumbersome to use because it required finding an equivalent back-EMF source on the AC-side of the inverter to make the rectifying mode work. It nevertheless allowed for real-time simulation of a VSI-based HVDC system including the start-up of the DC bus charging through an auxiliary diode bridge and emergency shutdown modes.

This paper presents an important improvement to this model that does not require the back-EMF source to be explicitly specified in the model. Several test results will be shown to demonstrate the applications of the model in Marine electrical power conversion systems.

II. SWITCHING-FUNCTION BASED 3-LEVEL INVERTER WITH HI-IMPEDANCE RECTIFYING CAPABILITIES

The 3-level inverter is based on previously published work [4][5][6] and has key properties like high impedance and rectification mode support, dead time simulation capability and interpolation of the output voltages based on time-stamping of gate inputs of the bridge.

The model is switching function-based and works in SimPowerSystems (SPS). It uses a SPS switch model in series with the standard switching function controlled voltage source to implement the high impedance mode. The model normally works as a standard switching-function when pulses are present. The model is then programmed to 1) detect a condition where gate pulses are blocked and 2) open the switches when the next current zero crossing occurs. Whenever the bridge is in state 2 (high impedance), the output voltage of the inverter is monitored and if this voltage (phase-phase) is greater than the total DC-link voltage (from negative to positive DC bus), 3) the corresponding inverters switched are re-closed and the algorithm goes back to step 2). In all case, the series switches are re-closed whenever pulses are sent again to the bridge.

III. VALIDATION TESTS

This section shows various tests made to validate the functionalities of the model. The offline validations were made by comparison of the proposed model results at 40 µs (unless otherwise mentioned) to the one obtained by an equivalent circuit modeled entirely in PLECS with the native 3-level NPC inverter model and simulated with a variable-step.

A. Tests made with RLE load model

The first model is a simple tri-phase RLE-load, without neutral point return and is shown in Fig. 1. In some rectification tests, a tri-phase voltage source can be put behind the RLE load. These tests were conducted in off-line mode.

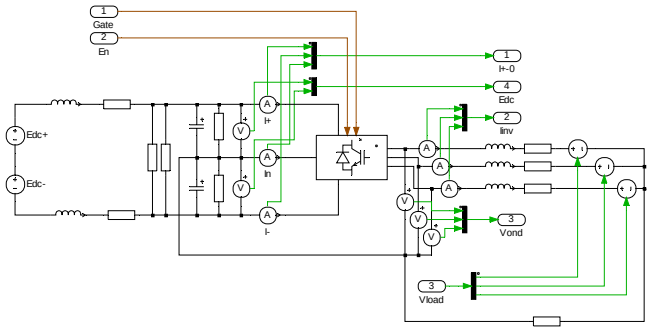

Fig. 1 RLE load driven by a 3-level NPC inverter

The model parameters are listed in TABLE I

TABLE I. RLE LOAD MODEL PARAMETERS

Componant	Value
Load resistance	5 Ω
Load inductance	10 mH
DC bus voltage (each level)	2333V
DC bus impedance	0.5 Ω, 1 mH
Discharge equivalent resistances	18.35 Ω
Inverter snubbers	None
PWM frequency	1587.3 Hz

1.1 Test with three phase load without neutral connect and 30% modulation index and 20µs dead-time

For this test, the inverter gate pulses are started at 0.01 sec with a toggle reference (zero sequence voltage), the modulation is applied at 0.02 sec with the modulation index to 30% and 50Hz of frequency. Then, the shutdown takes place at 0.05 sec. The voltage load is started at 0.06 sec .We have a step voltage in the range time between 0.08 sec and 0.1 sec. The dead time and the minimum pulse are set to 20µs.

Figure 2 and Fig. 3 show the input and output inverter voltages and currents for this test.

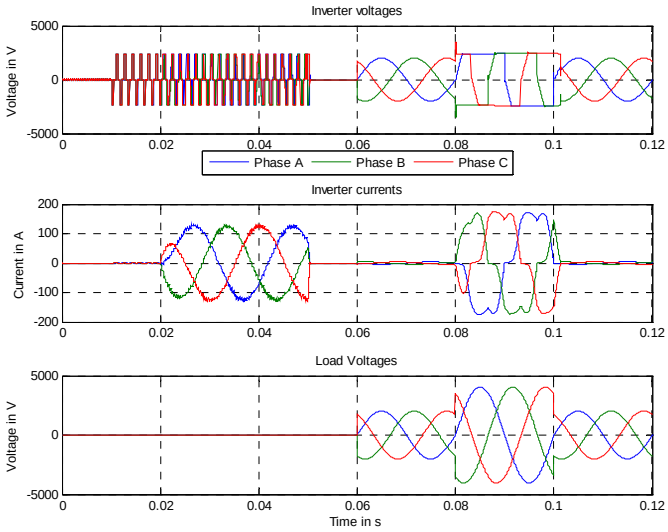

Fig. 2 Inverter currents, load voltages and inverter voltages for Test 1.

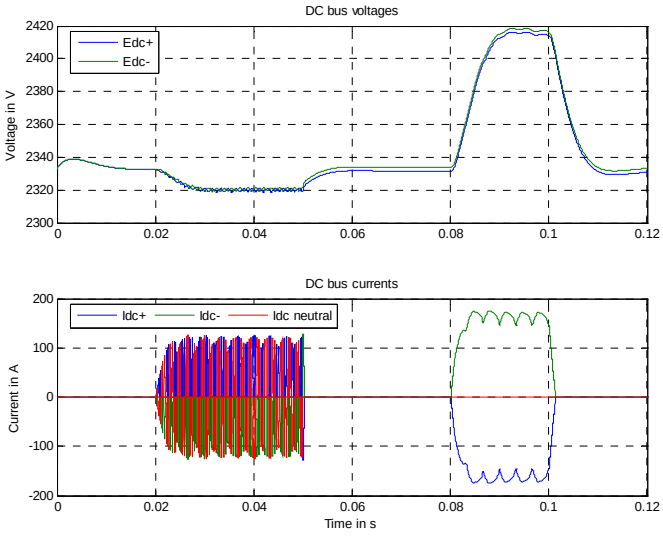

Fig. 3 DC bus voltages and currents for Test 1

1.2 Comparison between RT-LAB and PLECS with a zoom on index modulation step to 30%

Figure 4 shows the output current and voltage of the inverter. The difference between RT-LAB and PLECS in the phase 'A' current is mainly caused by the interpolation method of the proposed model.

Figure 5 shows the DC bus voltages, which seem qualitatively correct.

Figure 6 illustrates the DC bus currents. The difference between the traces is mainly caused by the sampling delay between the inputs and the outputs of the proposed inverter model.

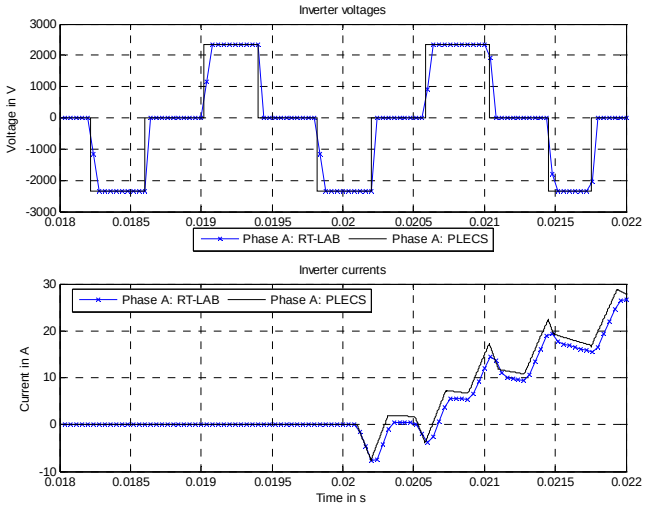

Fig. 4 Zoom of inverter voltages and currents for index modulation step to 30%.. Comparison between RT-LAB and PLECS.

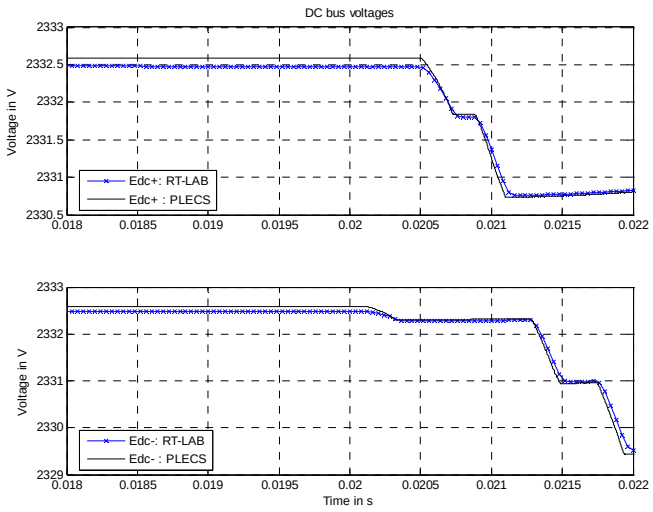

Fig. 5 DC bus voltages comparison between RT-LAB and PLECS, index modulation step to 30%.

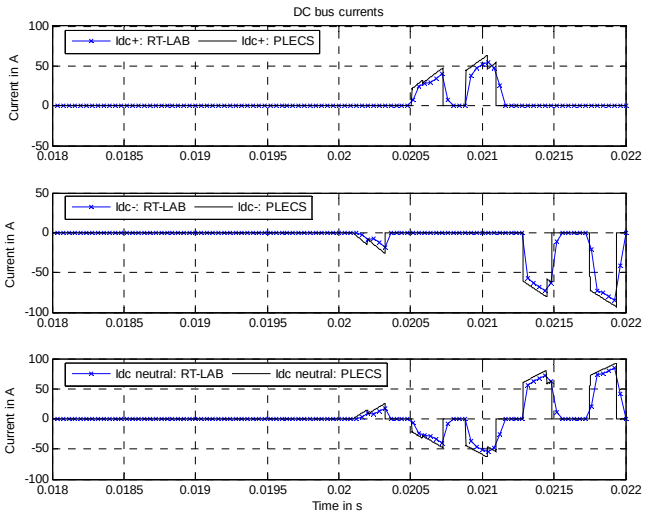

Fig. 6 DC bus currents, index modulation step to 30%. Comparison between RT-LAB and PLECS.

1.3 Comparison between RT-LAB and PLECS with a zoom on cut-off pulses and the Hi-impedance mode

Figure 7 shows the output voltage and current of the inverter. Figure 8 shows the DC bus voltages. The voltages are quantitatively correct.

Figure 9 shows the DC bus currents. Again, there is a sampling delay between the inputs and the outputs of inverter module. The Hi-impedance mode is qualitatively correct as currents drop to zero in that case.

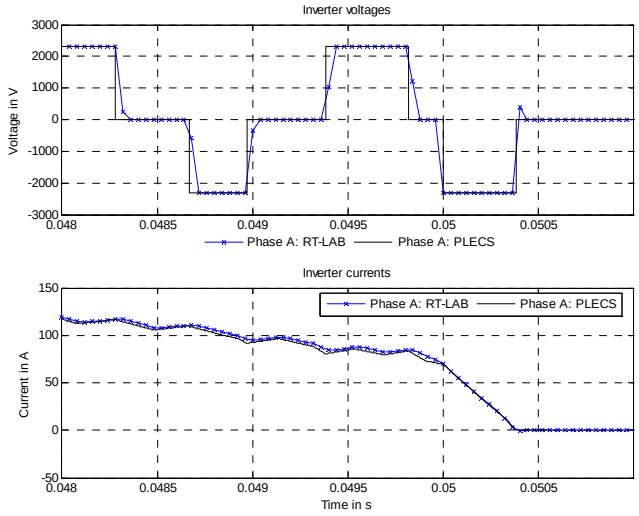

Fig. 7 Zoom at pulse cut-off of inverter voltages and currents. Comparison between RT-LAB and PLECS.

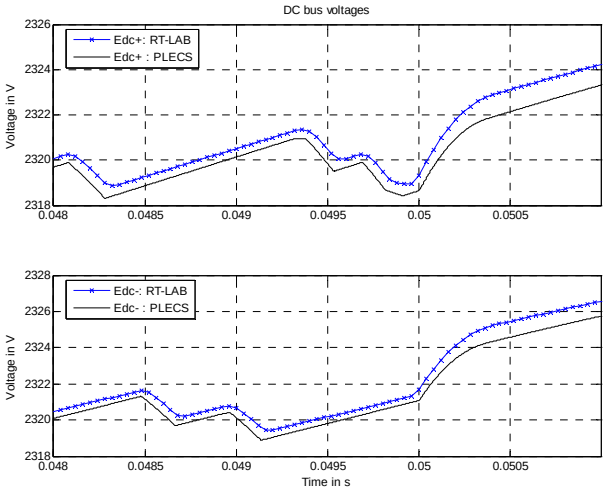

Fig. 8 DC bus voltages at pulse cut-off. Comparison between RT-LAB and PLECS.

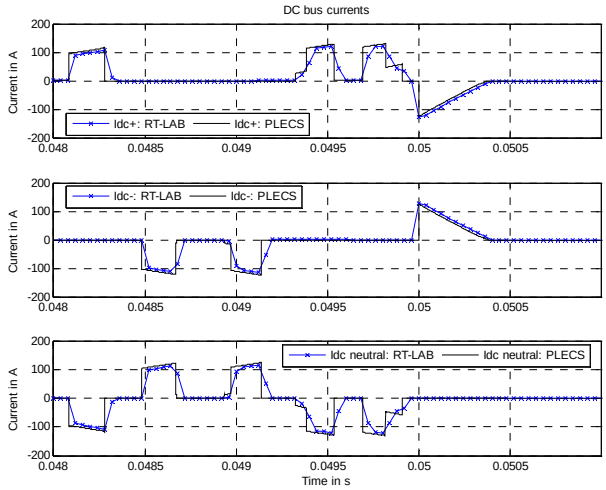

Fig. 9 DC bus currents at pulse cut-off. Comparison between RT-LAB and PLECS.

1.4 Comparison between RT-LAB and PLECS with a zoom on rectifier mode.

Figure 10 shows the output voltage and current of the inverter. The voltage spike of the proposed model, with regards to the PLECS reference, is caused by the detection of rectifier mode with two sampling delays.

Figure 11 shows the DC bus voltages. The voltages are quantitatively correct. Figure 12 shows the DC bus currents. Again, there is a sampling delay between the inputs and the outputs of inverter module.

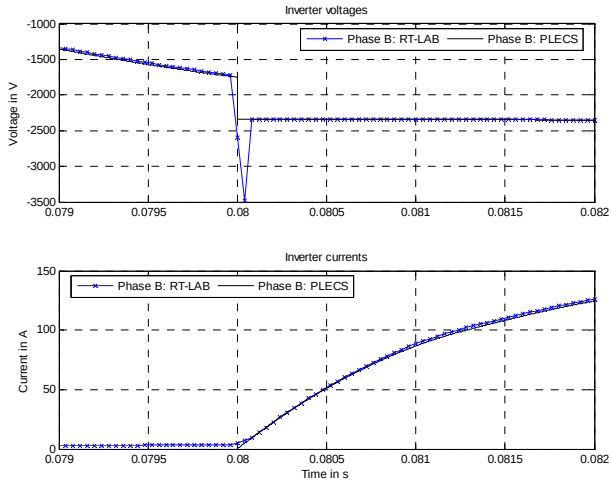

Fig. 10 Zoom of inverter voltages and currents at the start of the rectifying mode. Comparison between RT-LAB and PLECS.

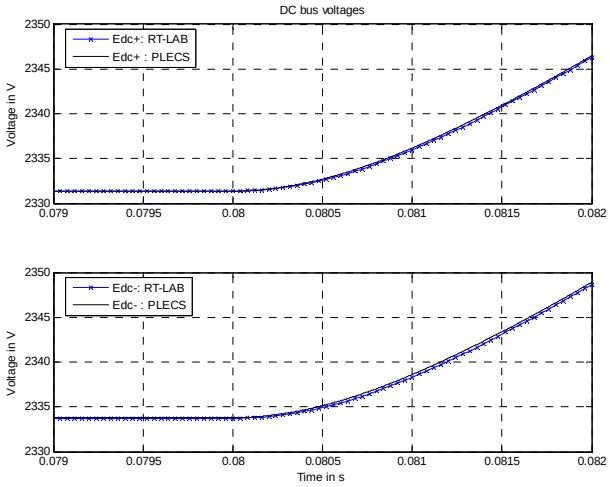

Fig. 11 DC bus voltages at the start of the rectifying mode. Comparison between RT-LAB and PLECS.

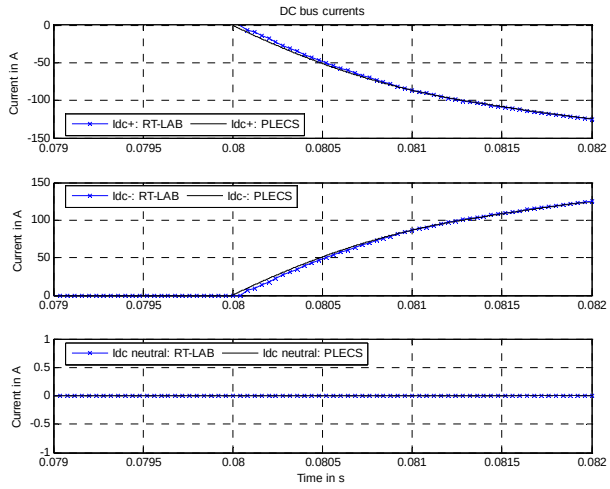

Fig. 12 DC bus currents at the start of the rectifying mode. Comparison between RT-LAB and PLECS.

1.5 Comparison between RT-LAB and PLECS with a zoom on the stop of rectifier mode.

Figure 13 shows the output voltage and current of the inverter. There is again a small difference between PLECS and the proposed model that do not affect the qualitative overall behavior in this mode. Figure 14 shows the DC bus voltages while Fig. 15 shows the DC bus currents.

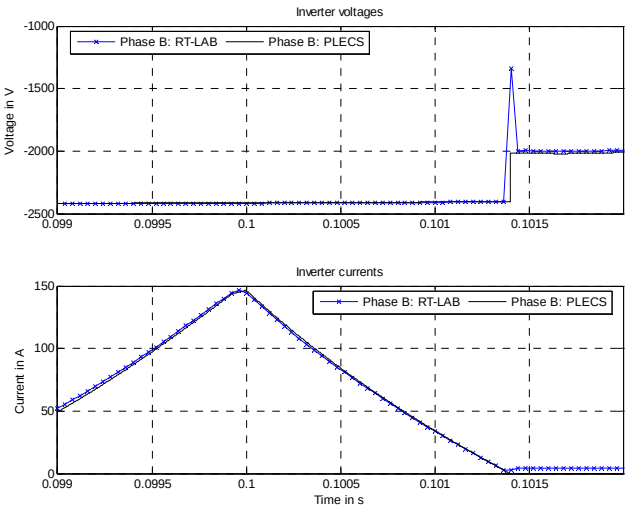

Fig. 13 Zoom of inverter voltages and currents at the stop of the rectifying mode. Comparison between RT-LAB and PLECS.

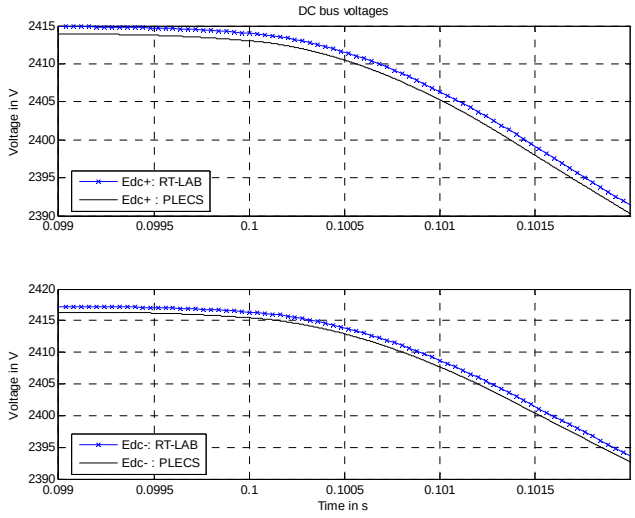

Fig. 14 DC bus voltages at the stop of rectifying mode. Comparison between RT-LAB and PLECS.

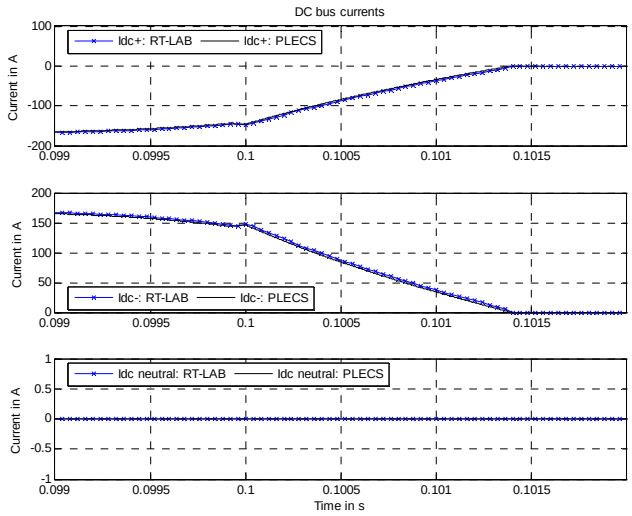

Fig. 15 DC bus currents at the stop of the rectifying mode. Comparison between RT-LAB and PLECS.

1.6 Analysis of off-line mode results

The analysis of off-line results is made here. Some differences can be observed between PLECS variable-step simulation and the proposed model. These differences are caused by the approach used to code the model. Basically, because the model is switching-function-based and separated from the main solver of SPS (used to model the series switch that is used to implement the hi-impedance mode) a sampling delay is always present in the solution. This is especially visible at the start and stop of the rectifying mode. Also, the model has a sampling delay between its input and output sides. This creates the delay that is visible on the DC bus voltages.

Finally, the model intensively uses interpolation because of its relatively large sample time (40µs). The effect of interpolation is clearly visible on the inverter output voltages, for example, where the voltage can have values different than the DC-link voltages when the conduction states are modified.

B. *Test made on marine drive system with AC-side 12-pulse rectifier 3-level induction machine drive with LRC-filter in HIL mode*

The simulation is done on a drive system composed of a transformer, a 12-pulse rectifier, a three-level neutral-clamped IGBT inverter drive and an induction machine powered through a filter. The simulation will include the AC-side and the mechanical behavior of the inductive machine.

The parameters used for this simulation are parameters from a real installation, a marine propulsion motor. The machine is rated at 12MW; 6600V; 13.13Hz. The number of poles equals 12, so the nominal speed is 131.3rpm.

The system is depicted in Fig. 16.

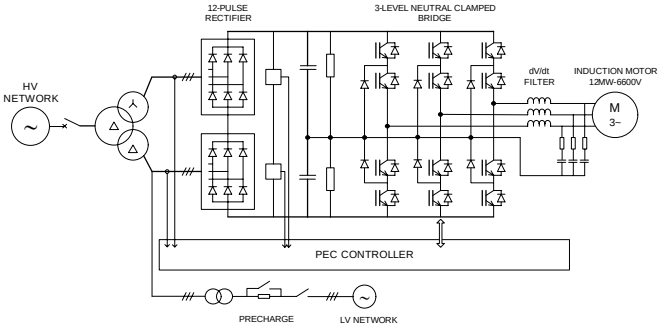

Fig. 16 Three-level IGBT inverter motor drive with LRC filter and 12-pulse AC-side rectifier

The Hardware in the Loop structure allows us to use the same command as in the project, by physically connecting our command system, called PEC (Power Electronic Controller). The PEC controller is composed of a VME rack with:

- PIB (Power Interface Board) for measuring the currents and voltages and generating the logical I/Os and the gates.
- CPU card for the drive control.

The PEC system allows the generation of the 12 IGBT command, based on the DC-bus voltage and the inverter currents. It also allows the sequential task, like the DC-bus pre-load or the drive starting.

The figures 17 to 23 come from a Converteam oscilloscope tool (Pertu tool) integrate in the controller.

Figure 17 shows the pre-load of the DC-bus and the pre-magnetizing of the motor. Figure 18 shows the start of the motor, with a constant rotor speed rate equal to 1.313rpm/s and a final value equal to 13.13rpm.

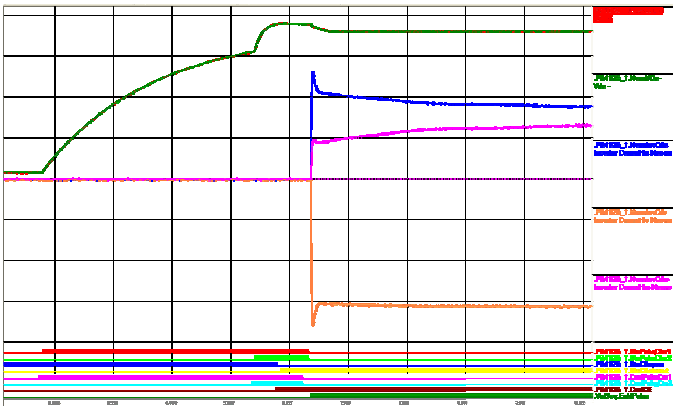

Fig. 17 DC bus voltage and inverter currents during the pre-charge of DC bus and the enable pulses.

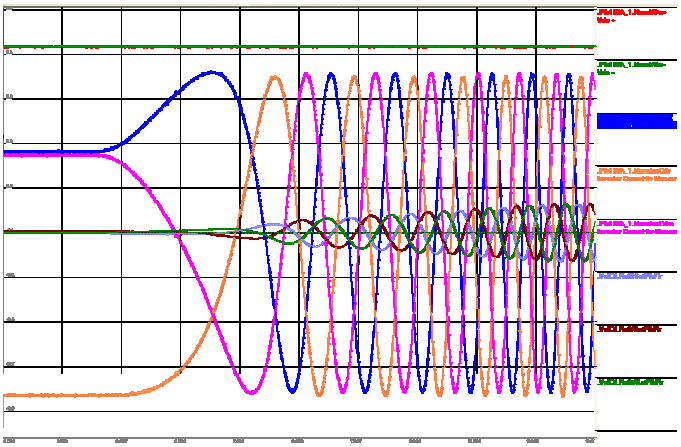

Fig. 18 DC bus voltage and inverter currents during the start of the induction machine in EVC mode.

An example of results obtained using a constant rotor speed equal to 45.95rpm is given in Figures 19 and 20, and equals 85.34rpm in Figures 21 and 22.

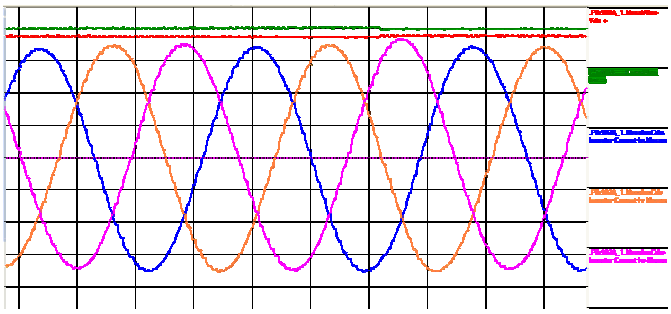

Fig. 19 Inverter currents and DC-bus voltages at rotor speed equal 45.95rpm

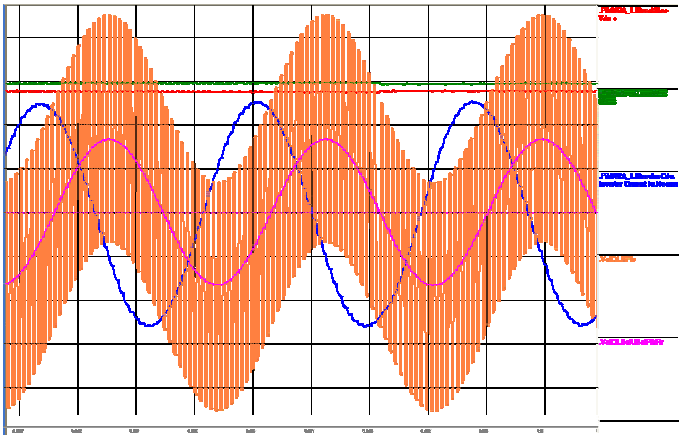

Fig. 20 A-phase inverter current and voltages with and without the homopolar component at rotor speed equal 45.95rpm

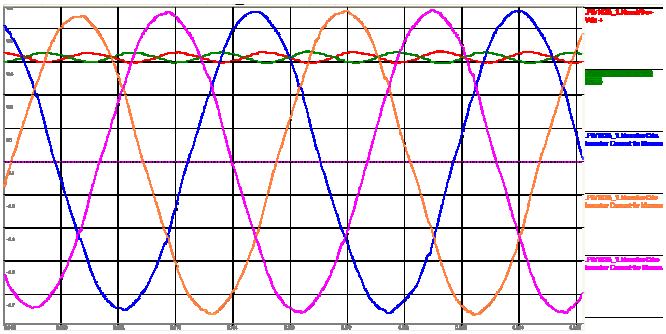

Fig. 21 Inverter currents and DC-bus voltages at rotor speed equal 85.34rpm.

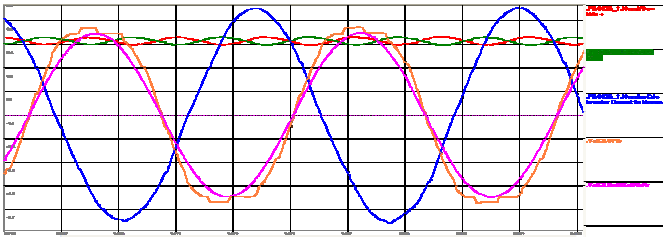

Fig. 22 A-phase inverter current and voltages with and without the zero sequence component at rotor speed equal 85.34rpm

In the case of the rotor speed equal to 45.95rpm (35% of the nominal value) the zero sequence component generated is called *Toggle*, which allows a better distribution of the IGBT losses. To the non-zero sequence voltage reference, a square wave is added. The square wave frequency is 200Hz, a 50% duty cycle and an amplitude equal to +/- 50%. The fundamental frequency equals 4.59Hz.

For the 85.3rpm rotor speed (65%), the command is called H3, which allows an increase in the amplitude fundamental voltage. In this case, the carrier frequency equals 400Hz, and a 20µs dead band is used for the IGBTs complementary command. The fundamental frequency equals 8.53Hz.

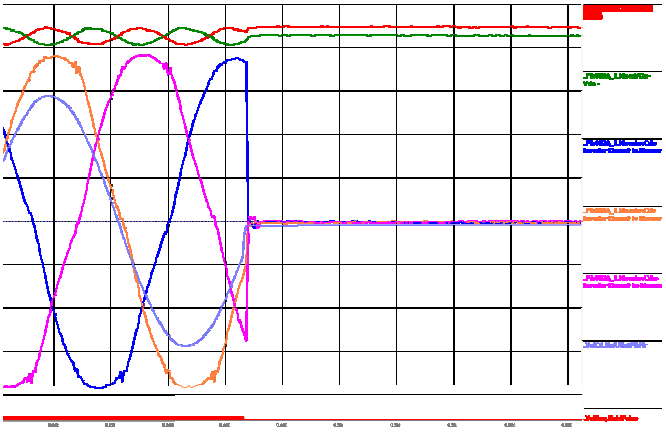

Fig. 23 Input currents, load currents and voltages for the disable pulses of inverter bridge

Figure 23 shows the behavior of the IGBT inverter during a cut-off of the IGBT's pulses. The pulse disabling forces all firing pulses to '0', turning off all IGBTs but allowing the diode to turn on, when required. The IGBT inverter works locally as a rectifier, which explains the small load of the DC-bus voltage.

The effect of the interpolation method used in the proposed inverter model can be seen in Fig. 24. For the purpose of the test, interpolation is disabled during the simulation at T=1 sec. For the test, the PWM frequency of the drive is 400Hz, the index modulation is 10%, a 20µs dead time is applied and the sampling frequency of the model is 25 kHz (Ts=40 µs). In addition and especially for this test, the controller dead-time compensation mechanism was disabled. This is observable by the small current distortion at zero crossing on the figure (before interpolation is disabled). On the figure, one can observe the increased distortion in the current and torque values when interpolation is disabled, and a change in current amplitude.

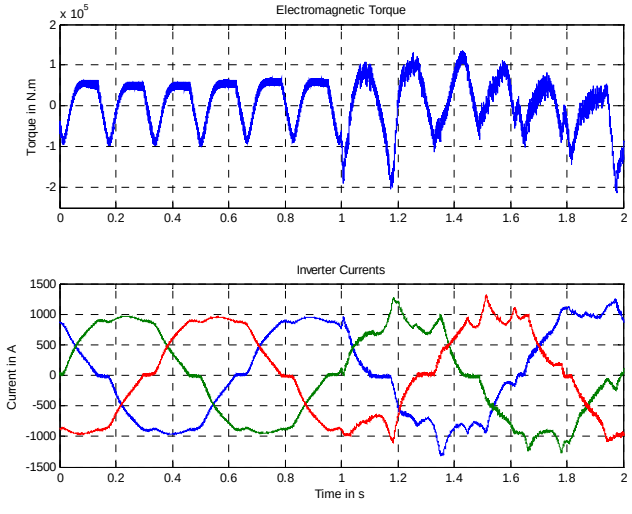

Fig. 24 Effect of interpolation on the accuracy

IV. REAL-TIME PERFORMANCE OF THE MODEL

The marine drive system with AC-side 12-pulse rectifier and induction machine load was simulated on the RT-LAB real-time simulator in HIL mode with the PEC. The results are shown in TABLE II. All the computing time given represents the maximum value measured. In this set-up, the 12-pulse rectifier is simulated on core #1 and the 3-level inverter and its load are simulated of core #2 for the simulator. The RT-LAB real-time simulator's six remaining cores were not used for these tests.

TABLE II. REAL-TIME PERFORMANCE ON 2.3 GHZ MULTI-CORE PCS.

Model	Computing time in µs	Real step size in µs (mean / max)	Configuration
High Power Three-level IGBT-Based Induction machine Drive	Core1: 13 Core2: 22	Core1: 40/44 Core2: 40/41	2 cores used. IOs: 12 TSDI 4 TSDO 9 AO, no AI

OUTLOOK

Several types of drives are expected to be simulated in short term in real-time using the 3-level inverter model presented in this paper. These include:

- High-speed induction machine drive (15000 rpm) with sinus filter, used in Oil & Gas applications
- Drive with Active Front End (AFE), used in network-connected applications.

Work is underway to validate the proposed inverter model in these various configurations. A new Converteam controller, named PECe, with an EtherCat link between the different boards will also be tested with these real-time models.

CONCLUSION

This paper has presented a real-time model of a 3-level Neutral-Point Clamped IGBT inverter. The model is suitable for Hardware-In-the-Loop testing of 3-level NPC inverter controllers and systems.

The paper also shows that the proposed model achieves a very high degree of accuracy when compared to regular SimPowerSystems or PLECS models. This has been shown in the paper by comparing inverter model responses in various modes of a simple 3-level inverter based drive in off-line mode.

The proposed 3-level inverter models have also been demonstrated to be compatible with HIL testing of PEC including difficult modes like emergency pulse shutdown or even stand-by mode of real controllers. These modes are important to correctly and thoroughly test physical controllers.

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