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An induction machine and power electronic test system on a field-programmable gate array

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Abstract

This paper presents a field-programmable gate array (FPGA) test system composed of an induction machine, configurable as a doubly-fed induction machine or squirrel-cage induction machine, with power electronic converter models suitable for virtual motor drive control development and testing. The IM model is designed so that all parameters can be modified online without stopping the simulation. The power electronic part is customizable using a variable topology FPGA solver called Electric Hardware Solver (eHS). Permanent magnet synchronous machine and switched reluctance motor drive FPGA models are also discussed. The system is designed for fast design iteration process by allowing circuit and parameter modification using a unique bitstream. The system allows control engineers to validate production controllers in real-time, using virtual motor drives. The paper also briefly explains permanent magnet synchronous motor drives and switched reluctance motor drive implementations on FPGA.

Keywords: Induction machine, induction generator, induction motor drive Hardware-In-the-Loop simulation, HIL simulation, DFIM, FPGA, eFPGAsim

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1. Introduction

The use of Field-Programmable Gate Array (FPGA) devices for the purpose of real-time simulation is an emerging trend for the Hardware-In-the-Loop (HIL) simulation. FPGA-based HIL is especially well adapted for high frequency PWM motor drives and power converters due to their very high sampling frequencies, typically in the nanoseconds range. HIL techniques are used for various applications [3] with the main objective of decreasing time-to-market of increasingly complex control systems and keeping the budget impact at bearable levels during the development phase, while running realistic tests in a safe environment using the actual controller hardware. The computational speed of FPGA, combined with their fast coupling capability with I/Os make them an excellent choice for such applications. In particular, FPGA-based models exhibit a very low HIL loop latency, sometimes a critical aspect in some high-end motor controller and protection system tests during normal and fault conditions.

Induction motor HIL simulation on FPGA is explained in the literature [1][2][9][10] using either fixed-point or floating-point format. A key aspect of HIL systems, in terms of industrial usability, is the ability to easily change model parameters and circuit topology. On FPGAs, this poses a serious challenge due to the long bitstream generation times.

In this paper, we present an FPGA test system composed of an induction machine (IM) along with power electronic converter models suitable for virtual motor drive control development. The IM model is designed so that all parameters can be modified online. The power electronic part is customizable using a variable topology FPGA solver called Electric Hardware Solver (eHS)[6]. Other FPGA configurations, with permanent magnet synchronous machine (PMSM) and switched-reluctance motor (SRM), are also briefly described.

The HIL system is designed for fast design iteration process by allowing circuit and parameter modification with a single bitstream. Both eHS and the IM are designed using floating-point arithmetic. The system allows control engineers to validate production controllers in real-time using a virtual drive, including the IM (and similarly for SRM and PMSM), with the connected power electronics converter.

2. Description of the eFPGAsim suite of FPGA models and solvers

The RT-LAB real-time simulator is designed to run models on FPGA and CPU. On the CPU, most Simulink models and toolboxes like SimPowerSystems are supported. On the FPGA, a customized suite of models and solvers was designed by OPAL-RT and is called e*FPGA*sim.

In e*FPGA*sim, the set of FPGA motors and inverter models available in 2015 are:

1- FEA-based Permanent Magnet Synchronous Motor (PMSM, IPM) [5][8]
2- Switched Reluctance Motor (SRM) [4]
3- Induction motor or induction generator (IM) [17].

FEA-based PMSM can simulate details such as cogging torque and saturation. Also available are more standard Linear DQ and Variable DQ (VDQ) PMSM models. VDQ is a DQ model that takes into account the saturation for all steady-state operating points. (By comparison, FEA-PMSM can handle transient saturation). Also note that PMSM covers special cases, such as BLDC (constant inductance matrix and/or trapezoidal flux) and Interior-Permanent-Magnet (IPM).

At the center of e*FPGA*sim is the Electric Hardware Solver (eHS), a general purpose electric system solver that can be configured to simulate user defined power electronic circuits without reflashing the FPGA card.

Also available in e*FPGA*sim are many types of custom-built converters, such as standard 2-level buck, boost, H-bridge buck-boost, and SRM unidirectional converters.

The e*FPGA*sim suite also allows the user to add custom VHDL or Xilinx System Generator code. These models' availability, as well as their connections, are customizable on a fixed FPGA bitstream that doesn't need to be recompiled. This e*FPGA*sim structure is depicted in Fig. 1.

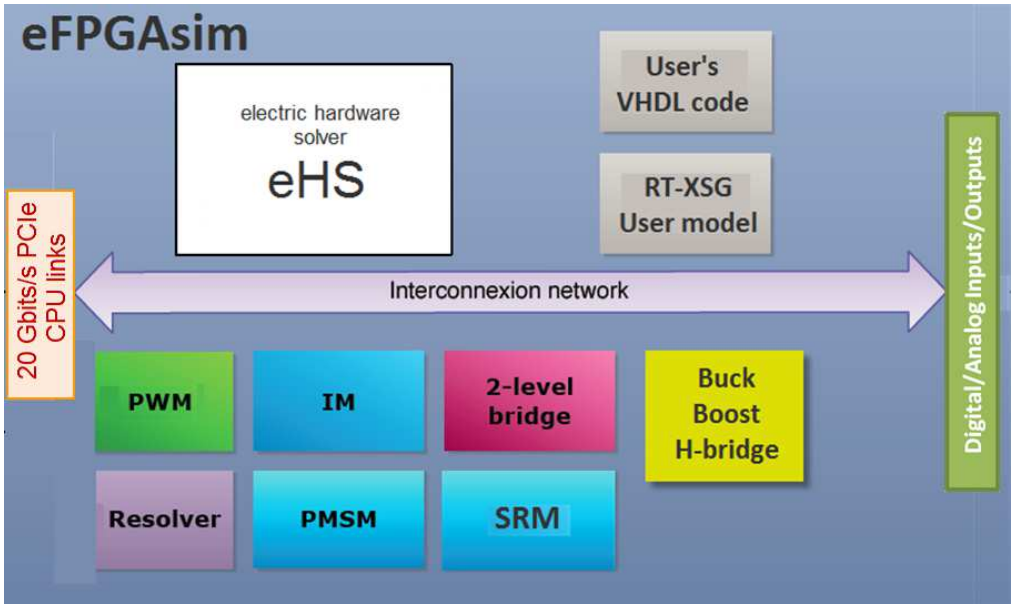

Fig. 1. e*FPGA*sim general structure

These models are all designed with floating-point arithmetic and the ability to change all parameters on-line. All these models have a sampling times below 500 ns and a total HIL latency close to 1 microsecond. Latency is defined here as the delay from the IGBT gate capture to the corresponding effect on the motor current at the analog output of the simulator. In essence, e*FPGA*sim is a set of precompiled modules, including eHS, that come in different configurations. Each configuration is a unique bitstream in which connections and parameters can be changed.

The availability of the induction machine in e*FPGA*sim was first described in [17]. In the next section, section, we describe the equations of the induction machine used in the e*FPGA*sim implementation; common e*FPGA*sim configurations involving PMSM and SRM are discussed in Section 5. Note that these configurations can be modified according to special requirements. Typically, a configuration comes with a user-chosen set of models and solvers that can be configured and inter-connected by the user.

2.1. Induction machine model on FPGA

An induction machine model with fixed d-q (Park) referential was used in this paper [11][13]. Phase domain voltage and current are therefore first transformed into the d-q domain using the orthonormal transformation using a fixed reference frame:

$$S = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \qquad (1a)$$

$$T = S.\sqrt{\frac{2}{3}}.\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \end{bmatrix} \qquad (1b)$$

with $\theta = 0$ for stator quantities and $\theta = -\theta_{rotor}$ for rotor quantities. The orthonormal transform is used to pass across the phase domain to the d-q domain. $V_{dq} = T.V_{abc}$ and $V_{abc} = T'.V_{dq}$

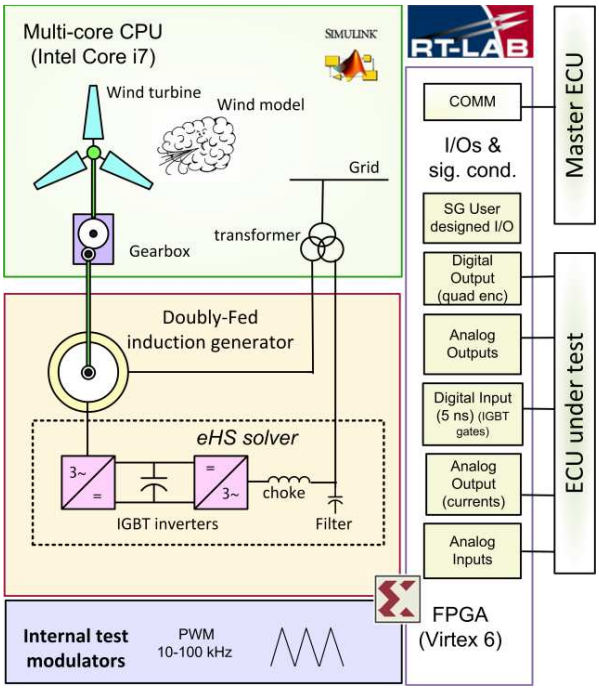

Fig. 2. Wind turbine and DFIM modeling on the CPU and FPGA of the RT-LAB simulator.

The machine equations are then equal to:

$$\psi'_{dq} = (RL^{-1} + \Omega).\psi_{dq} + V_{dq} \qquad (2)$$

$$I_{dq} = L^{-1}.\psi_{dq} \qquad (3)$$

With $V_{dq} = [V_{sd}\ V_{sq}\ V_{rd}\ V_{rq}]'$, $\psi_{dq} = [\psi_{sd}\ \psi_{sq}\ \psi_{rd}\ \psi_{rq}]'$ and $R = diag(-R_s, -R_s, -R_r, -R_r)$

$$\Omega = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega_e \\ 0 & 0 & \omega_e & 0 \end{bmatrix} \qquad (4)$$

ω_e is the electric frequency of the rotor ($\omega_e = pp.\omega_m$ with pp being the number of pair of stator poles and ω_m the rotor mechanical frequency). Also note that $L_s = L_m + L_{sl}$ (similarly for rotor), where L_{sl} is the stator leakage inductance.

$$L^{-1} = \frac{1}{L_r L_s - L_m^2}\begin{bmatrix} L_r & 0 & -L_m & 0 \\ 0 & L_r & 0 & -L_m \\ -L_m & 0 & L_s & 0 \\ 0 & -L_m & 0 & L_s \end{bmatrix} \qquad (5)$$

with R_s, L_s, R_r, L_r, L_m being the stator resistance, stator inductance, rotor resistance referred to the stator, rotor inductance referred to the stator and mutual inductance.

Electric torque is computed with the following formula (without the 3/2 term because of the use of the orthonormal transform in Eq. 1):

$$T_e = pp * (\psi_d i_q - \psi_q i_d) \qquad (6)$$

Figure 2 shows a typical configuration of the DFIM with common I/Os and CPU side of the simulator where complex Simulink models can be implemented in full synchronization with the FPGA side. The CPU side of the simulator will typically contain slower parts of the model, such as wind models, turbine and bearings, as well as the DFIM electric feeder circuit. Since we are looking for a simulation time step in the sub-micro-second range, the discretization of the induction machine is done with the Forward-Euler method, which is accurate enough at these discretization time steps.

The present IM model does not include a specific saturation or core loss methods but is designed for this purpose because all parameters of the DFIM equations are modifiable on-line, much like the Ω matrix that changes according to the rotor speed. An IM model with saturation and core loss is presented in [15].

2.2. Power electronic circuit simulation on FPGA

e*FPGA*sim has different modules to simulate power electronic circuits: eHS (Electric Hardware solver) and custom modules, as shown in Fig. 1.

The eHs module is designed to model complex drives such as multi-level, multi-phase drives or matrix converters for example. In the DFIM application of this paper for example, a back-to-back converter along with the filters and choke are implemented in the eHS solver of e*FPGA*sim. The eHS solver uses the Fixed Admittance Matrix Nodal Method (FAMNM) with Backward-Euler discretization. This module enables the implementation of *user defined topologies without bitstream modifications*. Avoiding regenerating new bitstreams for each new circuit topology or parameter is a key aspect of this technology because it greatly accelerates the development cycle (A Virtex-6 bitstream generation typically takes more than 1 hour with a modern computer).

As its name says, the FAMNM method is constructed around a nodal admittance solver in which the matrix is kept constant [12]. This is possible by modeling the switches as dual-state components: a capacitor of value *C* when the switch is opened and an inductor of value *L* when the switch is closed. The following condition:

$$\frac{C}{h} = \frac{h}{L} = g \qquad (7)$$

with the Backward Euler discretization rule and *h* being the sample time of the model makes the admittance matrix of the circuit constant. Trapezoidal rule results in a slightly different relation. Indeed, under these conditions, both inductance L and capacitor C states of the switches have the same so-called ‘discrete admittance’ (or conductance) value of *g* and the resulting admittance matrix of the model remains constant and can be pre-inverted before the real-time iterations, therefore greatly increasing simulation speed.

The sample time of the eHS-64 module can go from 150 to 500 nanoseconds, automatically determined according to the complexity of the circuit, giving an excellent resolution for the IGBT firing pulses, which are

directly connected to the FPGA in the RT-LAB architecture. The internal architecture of eHS is too complex to describe here and the reader is referred to [18] for more details.

Other custom modules such as 2-level inverter, SRM converter and buck, buck-boost, boost and H-bridge converters are also available. These modules are implemented using binary switch models (unlike eHS which uses an L/C switch model) and can be used as an alternative to eHS in special applications where the parasitic inductance/capacitance of the eHS solver are undesirable. These custom modules typically run with sample time close to 100 ns

2.3. Firmware support for eFPGAsim with eHS

All e*FPGA*sim models were implemented on the ML605 board with a Xilinx-6 FPGA chip. Base frequency of the Virtex-6 FPGA is 200 MHz. Kintex-7 and Virtex-7 FPGAs are also supported.

One eHS module can fit on a Xilinx Kintex-7 (version 325T) used in the OP4510 OPAL-RT real-time simulator along with a predetermined set of machines models (IM, PMSM, SRM). Two eHS modules can fit on the OPAL-RT OP7020 RCP/HIL Virtex-7 FPGA Processor Expansion Unit. Table 1 gives some sizing of the latest eHS-64 version. As switches are modeled as L/C elements, the maximum number of both switches and reactive elements is 168 and the number of switch can be 72 per core at maximum in eHS-64.

Table 1: eHS-64 characteristics on Kintex-7/Virtex-7

Parameter	Maximum number
Inputs	32
Outputs	32
Switches	72
Switches + L/C states	168
Max # of core on Kintex-7	1
Max # of core on Virtex-7	2
Sample time	150 ns to 2.56µs

3. Coupling between FPGA and CPU model subsystems on RT-LAB

While the DFIM and other machine models and power electronic converter models are implemented on the FPGA, they are also connected to the grid transformer and feeder circuit simulated on the Intel multi-core CPUs of the RT-LAB system. The two simulation domains (FPGA and CPU) are interfaced using the fast PCI Express 20-Gbits/s communication links.

The CPU side of the simulator can also contain mechanical models, like traction model of trains or wind equations in DFIM wind farm applications. The communication between the CPU cores and the FPGA is made synchronously at the (slower) CPU rate and enables full interaction of simulated models in both domains. It is also possible to acquire FPGA simulation data at the FPGA sample time (5-500ns).

3.1. Control system prototyping

Control systems can also be prototyped using Simulink control functions implemented on the standard INTEL CPUs and fast PWM function on the FPGA chips. This CPU-based rapid control prototyping (RCP) technique is very useful to design and test controller algorithms before their implementation on target micro-controllers or FPGA chips, which are more difficult to program than implementing a controller with Simulink.

4. Validation

In this section, we perform the experimental validation of the e*FPGA*sim induction motor configuration.

4.1. Squirrel-cage induction motor drive

The simulation model can be reconfigured to model a simple inverter-driven induction motor (IM) drive. In this set-up, the induction motor is directly driven by a 3-phase inverter, with both models on the FPGA. The mechanical load of the induction motor is modeled on the CPU side of the simulator.

The parameters for this motor, shown in Table II, are the ones of a drive in the MW range used in off-highway-vehicle and described in [7].

Table II: Induction motor parameters

Motor parameter	Value and unit
Inertia	12 lb.s^2
Stator leakage inductance	0.217 mH
Rotor leakage inductance	0.274 mH
Mutual inductance	8.617 mH
Stator resistance	9.3 mΩ
Rotor resistance	8.7 mΩ
Pair of poles	3

The simplest test case is to start the induction motor, directly connected to a 3-phase inverter drive. We run the test case and compare the results of the SimPowerSystems model at 1µs with the result of the FPGA-IM in e*FPGA*sim. In this case, the time step of the inverter is 150 ns and the IM runs at 300 ns. In Test #1, we energize the IM stator directly in 6-pulse mode at 1125 RPM. In Test #2, we change the modulation index from 0.7 to 0.8 at 3000 RPM. Other parameters are listed in Table III.

Table III: Test parameters

Test #1	
PWM frequency	680 Hz
Modulation	Null→ 6-pulse mode
Motor speed	1125 RPM
Slip	0.0625
Test #2	
PWM frequency	1200 Hz
Modulation	0.7 → 0.8
Motor speed	3000 RPM
Slip	0.1

4.2. Test #1:square-wave modulation

In this test, we run the induction machine at 60 Hz fundamental frequency on the stator and 1125 RPM rotor speed (slip=0.0625). The machine runs in 6-step mode in this test. (6-step mode is a mode in which the PWM inverter applies square-wave voltage to the stator. The name comes from the fact that in this mode, each of the 6 inverter switches is turned ON/OFF only once per stator electric turn.)

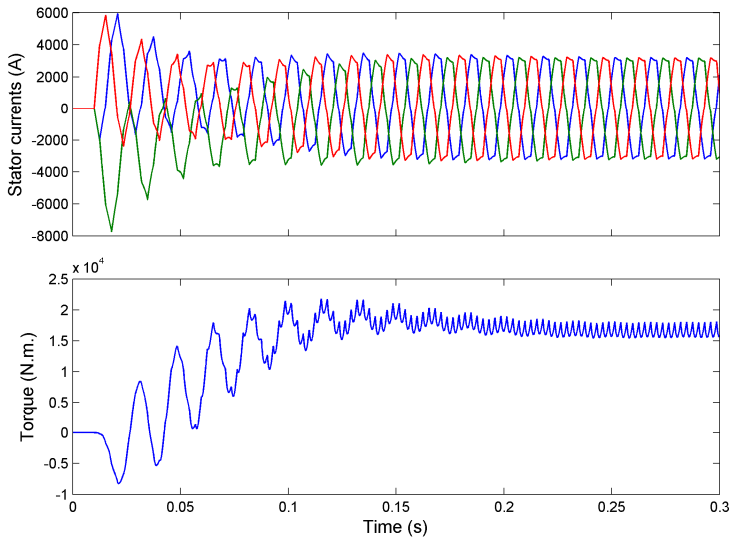

Fig. 3. Test #1: Current and torque for 6 step-mode @1125 rpm

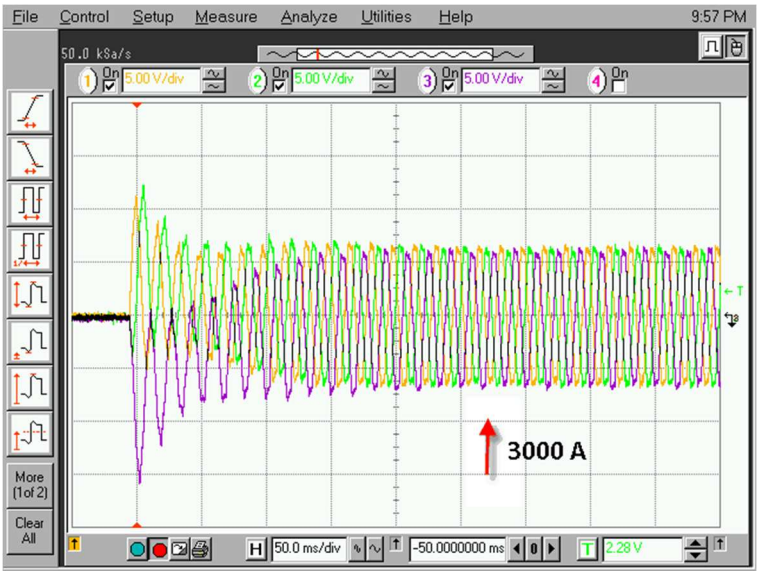

Fig. 4. Test #1: FPGA current captured on oscilloscope for 6-step mode @ 1125 rpm

The result of the Offline simulation (SPS @ 1 µs) is plotted in Fig. 3. They match the FPGA simulation results of Fig. 4 well. Energizing time was not the same on the two tests and therefore the initial transients differ a little bit. However, the steady state current is accurate and its shape has the recognizable 6-pulse shape as shown in Fig. 5.

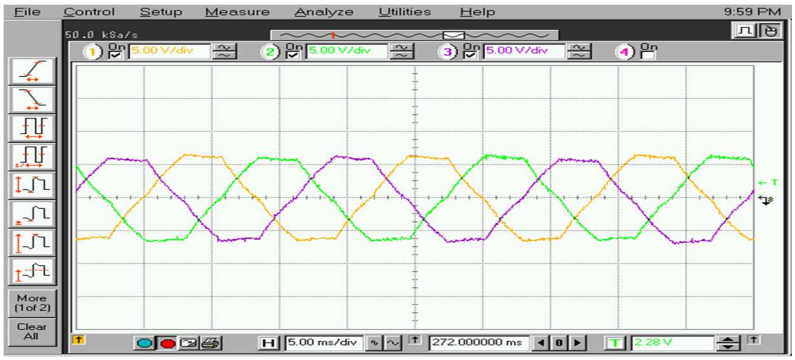

Fig. 5. Steady-state currents in 6-step mode on FPGA

4.3. Test #2: modulation index change

In this test, we run the induction machine at 120 Hz fundamental frequency on the stator at 2160 RPM rotor speed (slip=0.1). The PWM frequency is 1.2 kHz and in the test we change the modulation index from 0.7 to 0.8 with SPWM.

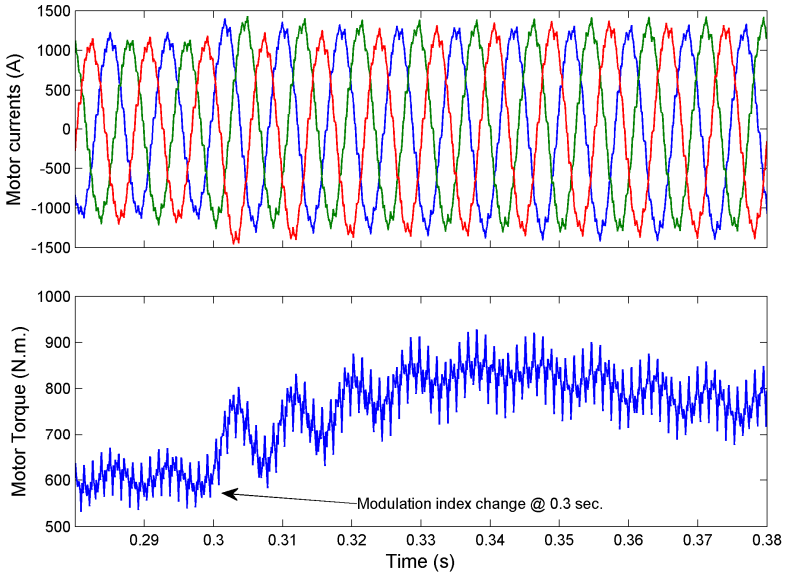

Fig. 6. Test #2 Currents and torque (offline results in SPS @ 1 µs)

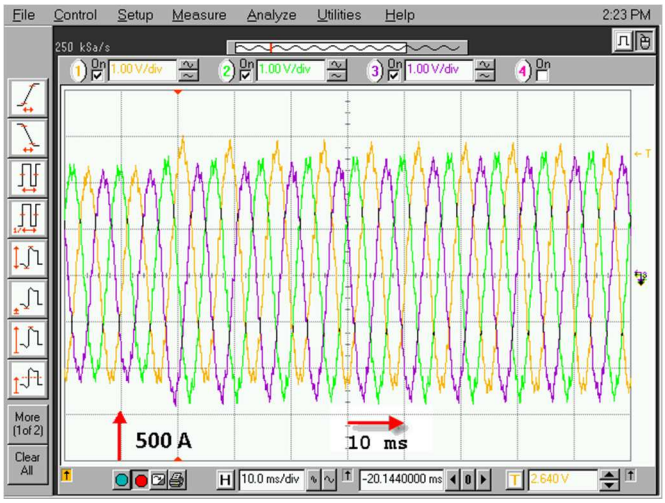

Fig. 7. Test #2: FPGA current captured on oscilloscope for PWM mode @ 2160 rpm

The result of the offline simulation is plotted in Fig 6. The FPGA currents, depicted in Fig.7, again match the offline results well. The slight imbalance of the currents, caused by the modulation index transient, is also present in the SimPowerSystems reference and fades away in both cases.

5. PMSM and SRM FPGA-Based Model Examples

In this section, we briefly present related motor drive models of e*FPGA*sim: SRM and PMSM.

5.1. Dual-PMSM with boost converter (Prius configuration)

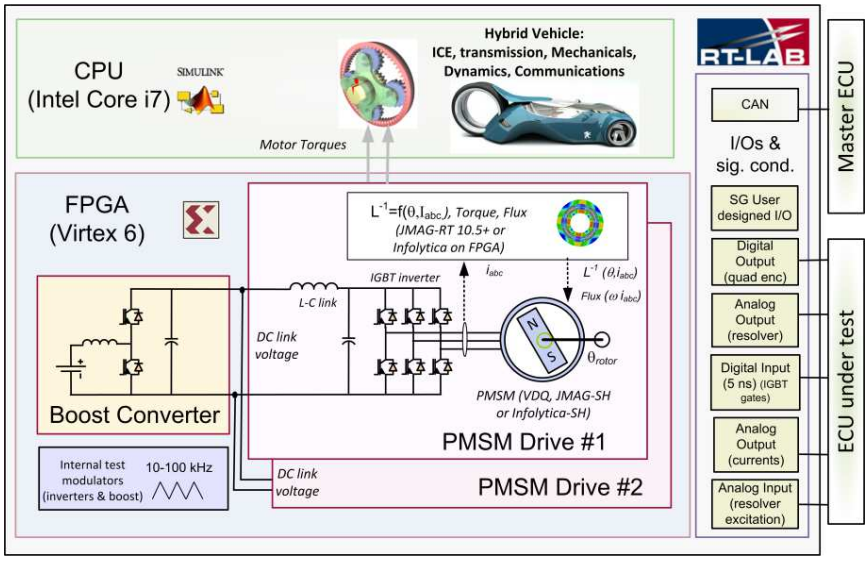

Fig. 8. Dual-PMSM and boost (Prius) eFPGAsim configuration

Figure 8 shows the e*FPGA*sim configuration is composed of 2 PMSM motor drives with Finite-Element Analysis data obtained from JMAG-RT and a boost converter[5][8]. The configuration also comes with resolver I/Os and internal test modulators. The latter are included to validate the model before HIL connection to the controllers. Other car subsystems, like transmission and mechanical systems, can be simulated on the CPU cores. Automotive communication protocols such as CAN or FlexRay are supported.

This configuration is notably used by Denso[5], an OEM for numerous car manufacturers and Ford[16]. This configuration allows many different types of faults to be made on the inverter IGBTs and diode. All model parameters can also be modified without building a new bitstream. As mentioned previously, such bitstream generation can be very long (more than 2 hours on a modern PCs), but e*PFGA*sim is designed to avoid these delays in the testing process.

5.2. SRM with buck-boost converter

In the field of HEV, PMSMs are the preferred choice of many manufacturers, mainly for efficiency reasons. Recently, the interest in switched reluctance motor drive has increased greatly because the high cost of rare-earth metals used in PMSM. SRM drives also benefit from low manufacturing costs, rugged construction and simplicity of controller design. Since the rotor has no windings and no magnets, it is a good candidate for drive operation at high speed and in adverse environments. As with IM and PMSM, a real-time simulator is the ideal tool to conduct research on this relatively new application of the SRM.

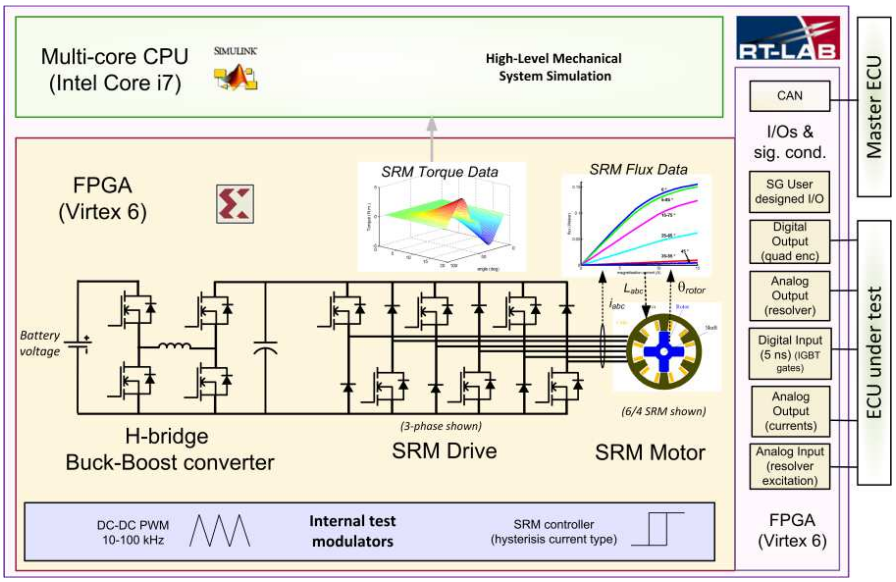

Fig. 9. SRM and buck-boost eFPGAsim configuration

Figure 9 shows the SRM configuration with a buck-boost H-bridge converter[4]. SRM data comes from JMAG-RT, Infolytica's MotorSolve or from the SimPowerSystems SRM model. The FPGA model also includes a resolver, quadrature encoders as well as a set of high speed digital input/outputs (10 ns resolution), analog inputs (2 µs update) and analog outputs (1 µs update). The bitstream also contains test modulators to allow for some model validation before connection to the controller under test in HIL mode.

6. Conclusion

This paper presented an induction motor test system based on FPGA technology. Excellent accuracy is obtained with FPGA modeling because of the very small time integration time step, combined with floating-point arithmetic. In the case of the IGBT converters, the high sampling rate also minimizes IGBT sampling errors and I/O latency.

The induction machine model along with the PMSM, SRM and eHS power electronic simulation modules are part of the OPAL-RT's e*FPGA*sim tool.

Tests were conducted in this paper to validate the induction machine model. They consisted in running the induction motor in a common traction application in which the motor is driven by a 3-phase IGBT inverter with a fixed rotor slip. The tests were accurate when compared to SimPowerSystems. Other motor types (switched reluctance and permanent magnet) were validated in other scientific papers[4][5] listed in the References section.

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Highlights

- We present induction machine model for FPGA simulation, suitable for Hardware-In-the-Loop tests
- We present a novel variable parameter and variable topology FPGA circuit simulation solver
- We also present other available motor (PMSM and SRM) on FPGA.
- All models and solvers are made in IEEE floating-point format and a unique FPGA bitstream is required