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Fault studies of MMC-HVDC links using FPGA and CPU on a real-time simulator with iteration capability

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***Abstract*— The detailed real-time simulation of MMC-based HVDC links is one of the most challenging tasks in power system validation today, requiring the combined use of CPU and FPGA technologies. The inclusion of surge arresters in the real-time fault tests further increases the difficulties because of the highly non-linear characteristics of such protective devices. In this paper, the OPAL-RT digital real-time simulator (DRTS) with the iteration capable State-Space-Nodal (SSN) solver is demonstrated to be accurate in such fault testing conditions. Two test cases are used for this purpose: an MMC-HVDC link based on the 401-level France-Spain link and a 271-level MMC system working in STATCOM mode.**

***Index Terms*—Real-time simulation, Iterations, MMC, SSN, HVDC, iterative methods, FPGA, STATCOM.**

I. INTRODUCTION

Modular Multilevel converter (MMC)-based High-Voltage Direct Current (HVDC) is a rapidly emerging technology for DC current transport. MMC are voltage source inverters, so they can minimize filtering requirements and add flexibility to the active/reactive control of the DC links. MMC HVDCs have the advantage of being very reliable and maintainable by their modular nature: the links can continue to work correctly when a module fails and even allow the replacement of this module without shutting down the link. This is an important issue for sites that are difficult to access, like off-shore wind-farms [1]. One other advantage of MMC-HVDC, over more traditional thyristor valve HVDC systems, is that they don't require the AC grid to be working (i.e. can operate during a grid black start) and can support AC voltage level on the AC side when needed, used as static compensators (STATCOM).

Hardware-In-the-Loop (HIL) MMC simulation is still a challenge as of 2016. Due to their complexity and highly-redundant structure, MMC converters are usually simulated in real-time with a combination of Field Programmable Gate Array (FPGA) and CPU core computing engines. Using HIL, MMC systems and their controls can be tested and validated, in normal and faulty states, before commissioning. [2][3][4][5][6][7][12][17][18][19]

This paper presents a real-time MMC-HVDC real-time simulation test bench designed for validation of all levels of controls in such systems.

Three tests cases are presented in this paper. The first case is inspired on works previously presented on the INELFE link in [4] and [5]. In [5], for example, the authors studied the impact of iterations in real-time but used a reduced cell equivalent MMC model runnable on the Hypersim simulator CPU's cores. In this work, a full model of MMC is used (400x6x2=4800 cells) and run in real-time on the DRTS. The second case is based on a large MMC multi-terminal HVDC system [17][18] in a set-up where an MMC station, with opened DC-link, acts as a STATCOM device on the AC grid.

In both cases, MMC circuitry and I/Os are implemented in a Virtex-7 field-programmable gate array (FPGA) and the rest of the power systems on CPUs, using OPAL-RT Technologies' e*MEGA*sim digital real-time simulator (DRTS) . The MMC valves are solved with a time step of 500 ns, while the grid is solved in parallel CPUs using the iterative SSN solver, with a typical time step of 25 microseconds.

This paper will demonstrate the importance of using an iterative real-time solver such as SSN when performing MMC fault testing and this is demonstrated for both configurations.

II. MMC CONVERTERS

The most common MMC configuration is composed of serial stacks of half-bridge cells (HBC), depicted in Fig. 1 A real HBC is composed of 2 IGBTs with anti-parallel diodes and a capacitor, together with a thyristor and by-pass switch, the two latter being used only in fault modes.

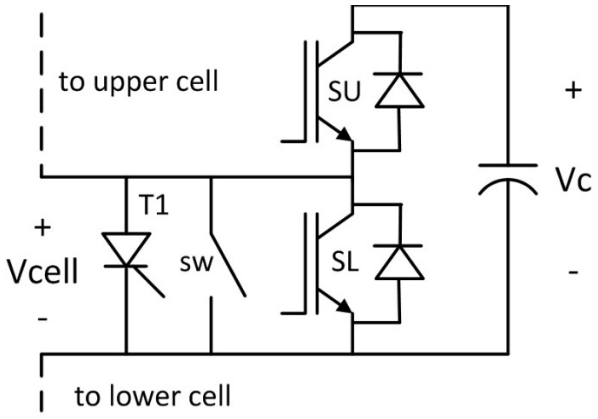


Fig. 1 One half-bridge MMC cell

By acting on the two IGBTs (SU and SL in the figure), the cell voltage is made either 0, or V_c, the capacitor voltage. This gating action also controls the current entering the capacitor and therefore its voltage. By controlling the HCB cell voltages of the stack, one can control the total arm voltage between 0 (when all HBC voltage=0) and *nbc**V_c (when all HBC voltage = V_c with *nbc* being the number of cell in the stack). Note that all the HBC may have different capacitor voltages and one of the primary control objectives is to maintain these capacitor voltages to some prescribed and equal value.

Other MMC configurations exist, such full-bridge MMC composed of 4 IGBTs per cell, in which added cell complexity enables more voltage levels per cell.

A. *MMC models for real-time simulation*

MMC circuits are challenging, when it comes to real-time simulation, due to their intrinsic complexity. Many methods can be used to incorporate MMC into real-time simulations, using CPUs and/or FPGAs.

1) *CPU only solution*

A common MMC model uses binary switch models for IGBT and diode, and methods to reduce all modules of an MMC arm to a Thevenin or Norton equivalent. Up to a total of about 500 cells can be completely run on CPUs using a nodal admittance method [13]. The method is well tailored for PWM-type MMC converters [15], such as the configuration to be used in The Northern Pass project between Quebec and New England. PWM-type MMC systems have much fewer voltage levels than standard MMC, in which each cell is activated one time per power cycle at maximum, but compensate this by using PWM modulation at each level used.

In this approach, the method consists in:

a- Computing all MMC capacitor cell voltages according to the current direction and IGBT gate level.

b- Dynamically computing the Thevenin equivalent of each MMC arm or cascade based on the switch conduction state and capacitor cell voltages.

The arm Thevenin equivalent is used by the SSN solver to compute the arm voltages and currents. In turn, these currents and voltages are used to determine the individual cell voltages, without delays. In this case, each MMC arm is really distinct 'SSN Group' in the global SSN algorithm depicted in Fig. 3

2) *Combined CPU-FPGA solution*

With MMC systems that have more than 100 cells per arm, it becomes more practical to use FPGAs to compute a large part of the MMC equations. In HIL testing also, FPGA are usually required at the I/O connection points and FPGA pre-processing of MMC equations becomes even more advantageous [14] [16]. For one HVDC link similar to the INELFE link, the number of I/O signals is greater than 10,000[3], for example. In one method using FPGA, the calculation algorithm is done in the following way:

a- Compute all capacitor cell voltages on FPGA according to the current direction and IGBT gate level.

b- Total cell voltage, including IGBT and diode voltage drops are sent to the CPU for incorporation as controlled voltage source into the global SSN solution.

c- Real diodes on the CPU are used to simulate the natural rectification mode.

Fig. 2 shows one cell equivalent model during a specific mode where the top IGBT is ON and the bottom one is OFF, for both current directions. Similar configurations are derived for other IGBT conduction states. Since all MMC cells are in series, current direction is unique for all cells in an arm and the total of a cell's equivalent voltage (V_c and V_{fd} in the figure) is transferred to CPUs for inclusion in the global SSN solution. Note that in this configuration, there is one step delay between the CPU and FPGA solutions. The delay is not a problem in active mode because of the low impedance of the branches. Diodes D1 and D2 are the equivalent diodes placed on the CPU to emulate natural rectification, thus this mode is computed *without algorithmic delays*.

Also note that the thyristor and bypass switch are not modeled separately; the lower IGBT action can correctly mimic their bypass effects in simulation. FPGA also have the purpose of routing the MMC cell gate signals to the CPU-side of the HIL simulator.

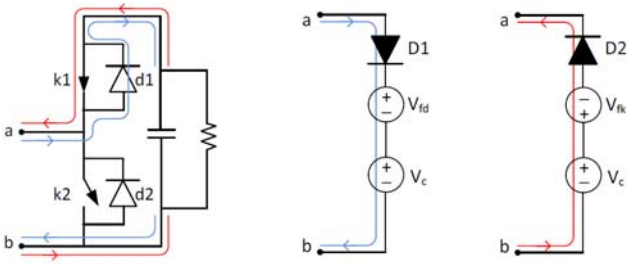


Fig. 2 FPGA-type MMC cell modeling. left) cell circuit middle) equivalent model for positive current. right) equivalent model for negative current.

III. SSN ITERATIVE SOLVER

The State-Space-Nodal (SSN) solver [8] is a nodal admittance based solver for power systems with iteration capability for surge arresters [9]. SSN uses state-space defined partitions instead of a fixed set of RLC branches that allow the user to control the size of the admittance matrix.

The SSN algorithm with iteration capability is depicted in Fig. 3 The SSN algorithm is essentially similar to classic EMTP algorithms with the following differences:

1- Branches are generalized to groups (or partitions). These are multi-terminal branches defined by the user.

2- Partitions are described by state-space equations which can be discretized by any matrix exponential function (see [11]).

3- SSN partitions are computed in parallel without delays. This 'parallel-in-step' capability of SSN enables it to simulate very large power systems [11].

4- Each partition performs internal iterations to verify consistency of the equation within the group in case of switching events with dependencies (ex: IGBT/diode)

5- Surge arresters (MOV) and distinct switches (not part of user-defined SSN partitions) are globally iterated around the global nodal voltage solution. After the YV=I solution, MOV and switch segment validity is verified and, if not valid, the segment is changed and the nodal voltage solution is computed again.

Concerning the 'parallel-in-step' capability of SSN, one should note that both companion and state update parts of the classic nodal admittance method (Fig. 3 parts of the algorithm before and after the YV=I steps) are really 'for' loops. These 'for' loop can be done in parallel effectively in SSN because the SSN partitions are big enough to 'beat' thread communication losses of modern PCs.

It should also be noted that recalculation of the nodal voltage solution after a MOV/switch segment change require a re-factorization of the admittance matrix. For this reason, the algorithm is designed so these MOV/Switch nodes are at the bottom-right of the admittance matrix.

One should also recognize that the most computer intensive part of the classic nodal admittance method is the *YV=I* part, even when not considering iterations, because the factorization of the admittance matrix is an $O(r^3)$ problem, where r is the rank of Y. In SSN the user to control the size of Y by the selection of the groups/partitions. (Nodes of Y are the connection points of the various partitions in SSN).

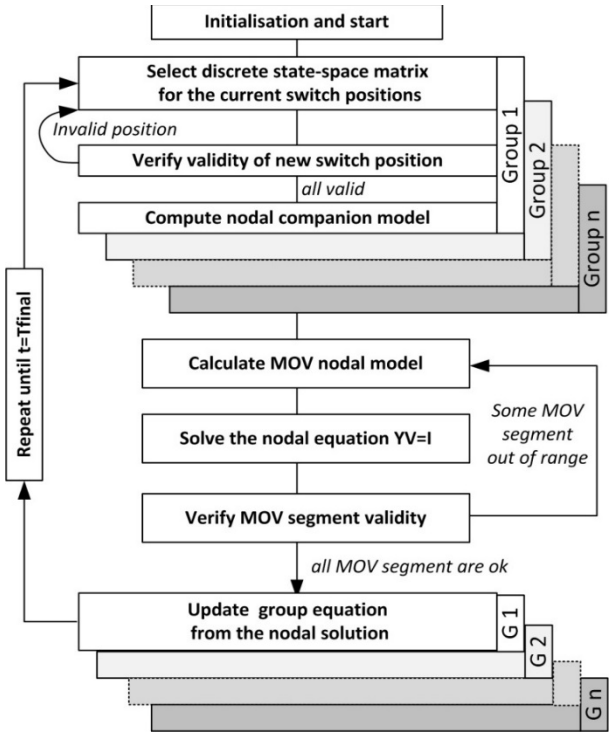


Fig. 3 Iteration capable SSN algorithm

IV. THE FRANCE-SPAIN MMC-HVDC LINK

The France-Spain MMC link [5] is used as a basis in this section to conduct fault studies using the e*MEGA*sim DRTS.

The France-Spain link is a 2,000 MW interconnection composed of 2 parallel HVDC-VSC links including 4 XLPE cables (64.5 km long each), for transmitting power between the 2 converter stations [4][5]. In this work, we use only one of the 2 links. A single line diagram of one (1) link of the full France-Spain interconnection is depicted in Fig. 4 with major parameters described in TABLE I. We refer to this model by the acronym **FS1** in the rest of this paper.

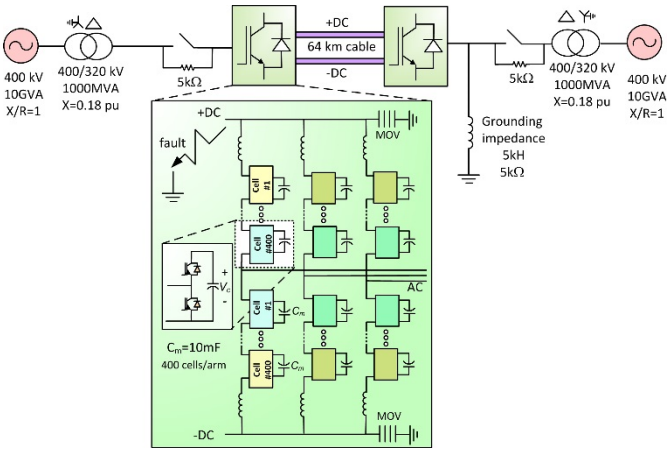


Fig. 4 ***FS1*** MMC-HVDC link used in this work

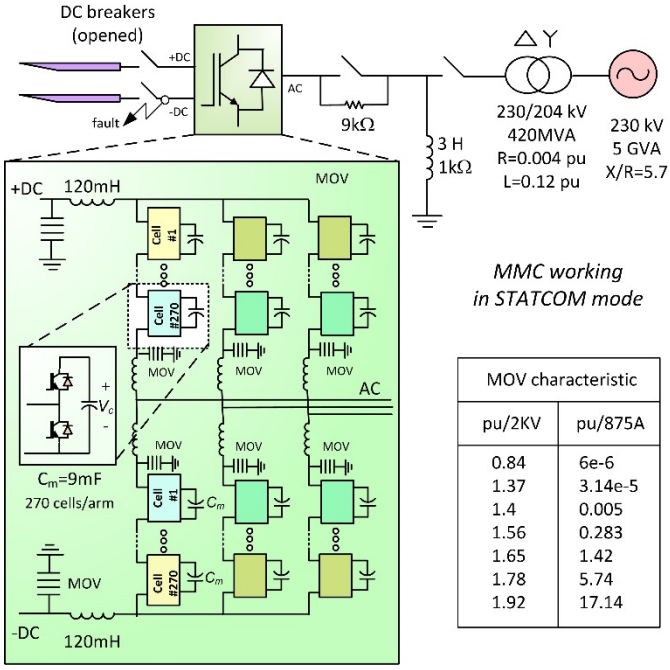
TABLE I. PARAMETERS OF FS1 HVDC-MMC LINK

Parameters	**Values**
Transformer voltage, power and impedance	400/320 kV, 1050MVA, 0.18pu, 50 Hz
MMC grounding impedance	5000 H 5000Ω (unfaulty side only)
Source short-circuit level	10000 MVA
Limb inductance	48.9 mH
Module capacitance	10mF
MMC level number	401
Insertion resistances	5000 Ω
Line length	64km
MOV voltage/current points [pu/290kV, pu/1.724kA]	{1.51/0.00002, 1.58/0.0046, 1.72/0.257, 1.82/1.3, 1.96/5.2, 2.70/52, 2.95/ 209}

The line model used in FS1 is of Bergeron with losses type, with RLC evaluated at 0.1 Hz, which is not the most accurate model for cables but provides the best calculation performance. Surge arresters are normally located on the DC and AC sides of the converters. In our simulation cases, we only put surge arresters at the DC line connection point, as depicted in Fig. 2 The MOV is modeled by a set of linear segments, with end points given in TABLE I. When a DC fault occurs at the terminal of this converter, a pole-to-ground overvoltage on the healthy pole can be observed due to the quasi-floating connections caused by the delta connection of the transformer.

V. THE ZHOUSHAN STATCOM-MMC

In this section, we describe a 271-level MMC system configured for STATCOM operation, as specified for the factory acceptance test of an Opal-RT's client in the Zhoushan region in China. The MMC-STATCOM is part a multi-terminal HVDC system and has its DC breaker opened in our case, disconnecting the MMC station from the other stations [17][18]. In this configuration, it is used to stabilize the AC voltage level, acting as a STATCOM. This model is named **ZS1** hereafter and is depicted in Fig. 5 with all relevant parameters.



MOV characteristic	
pu/2KV	pu/875A
0.84	6e-6
1.37	3.14e-5
1.4	0.005
1.56	0.283
1.65	1.42
1.78	5.74
1.92	17.14

Fig. 5 MMC model ZS1, STATCOM mode, with all parameters

VI. REAL-TIME SIMULATOR SET-UP FOR MMC-HVDC

The e*MEGA*sim DRTS uses a Virtex-7 FPGA to simulate the MMC converters: 3 arms each with 400 HBC per arm for a total of 4800 HBC for the FS1, and 1620 HBC in total for ZS1. A pair of 10-ten core microprocessors to simulate the rest of the network; this part running with the State-Space-Nodal (SSN) solver [8]. In our tests, only 4 out of the 20 available cores were used.

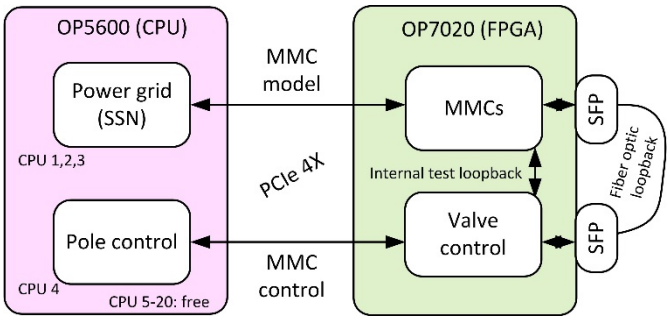


Fig. 6 MMC-HVDC link task distribution on CPU and FPGA computational engines

The pole control and power systems, including MOVs, are simulated OPAL-RT's OP5600 real-time simulator CPUs, while the MMC cells (up to 4800 HBC in our case) and the low-level valve controls are embedded in OP7020 Virtex-7 FPGA Processor Expansion Unit, as depicted in Fig. 6

A. I/O connections

The e*MEGA*sim simulator is designed to simulate large MMC systems and communicate a large number of signals with external devices through fiber optics or copper wires. Since an industrial controller is not available for this case study, an internal controller is used. A PCIe x4 (20 Gbits/s) cable connects the CPUs and FPGA systems. For the physical layer, the real-time simulator is equipped with small form-factor pluggable (SFP) optical transceivers. Each SFP can plug in one pair of optical fibers for bi-directional communication. In the data link layer, the simulator supports high speed communication protocols, such as the Xilinx LogiCORE™ IP Aurora, or gigabit Ethernet. The signals between the MMC and the actual MMC controller can be routed through protocol driver and optical fibers. In the tests made in this paper however, these signals are routed internally in the FPGA.

The OP7020 Virtex-7 FPGA Processor Expansion Unit can simulate up to 6000 half-bridge cells as of 2016, along with their low-level controls. This is suitable for all industrial MMC configurations known to date.

VII. REAL-TIME SIMULATION RESULTS

A. France-Spain MMC-HVDC

Fig. 7 presents the result of a pole-to-ground fault made on one FS1 link simulated on e*MEGA*sim with the fully detailed MMC converters (2x 2400 HBC) simulated in the Virtex-7-based OP7020 simulator. In the figure, we can observe:

1- The DC-link natural rectification charging

2- Current regulation is started at around 8 sec.

3- The fault is applied at 15 sec.

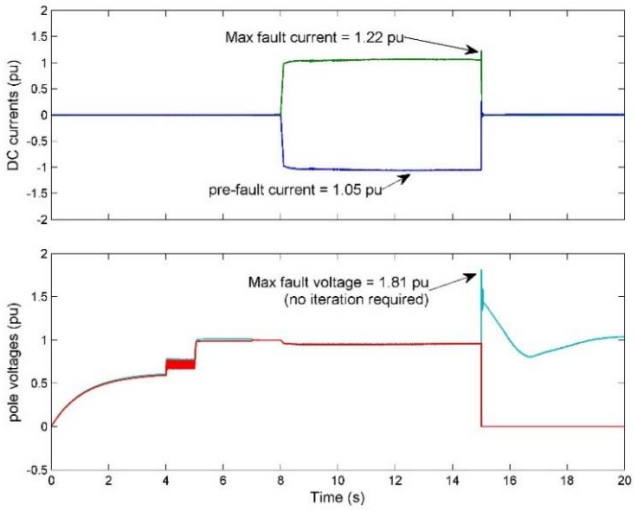


Fig. 7 FS1 pole to ground fault; real-time results of eMEGAsim & Virtex-7 FPGA

The MMC faulted side converter is then blocked 6.18 milliseconds after the fault, followed by the opening of the AC circuit breakers 70 milliseconds after, on both sides of the link.

During such a fault, the healthy pole voltage could rise to 2 PU if it was unprotected, because the circuit located on the delta side of transformers are essential floating, with a very large grounding impedance. As seen in Fig. 7 the MOV limits the healthy pole overvoltage to 1.81 PU, with and without iterations.

The result of the pole-to-ground fault of the FS1 case show that no iterations are required to obtain accurate results at the CPU simulation time-step of 25 µs.

B. FS2 model: FS1 model with 100 mH smoothing reactors and MOV set at 85% of nominal protection voltage

In this section, we modified the FS1 model case in the following ways:

- added 100 mH smoothing reactors at the line ends
- MOV protection voltage set to 85% of original values

This model is named **FS2**. Fig. 8 shows the pole voltage and current during start-up and the fault for the FS2 model. The fault is applied at the MOV connection point, between the MMC arms and the 100 mH smoothing reactor. At the instant of the fault, the healthy pole voltage rise to 1.60 PU in the simulation with 1 iteration while it rises to 1.69 PU without iteration. In the figure, the zoom shows clearly that without iterations, the voltage rise was too fast for accurate simulation at the selected time step of 25 µs. Pole currents this time rise to 2.06 PU in all cases.

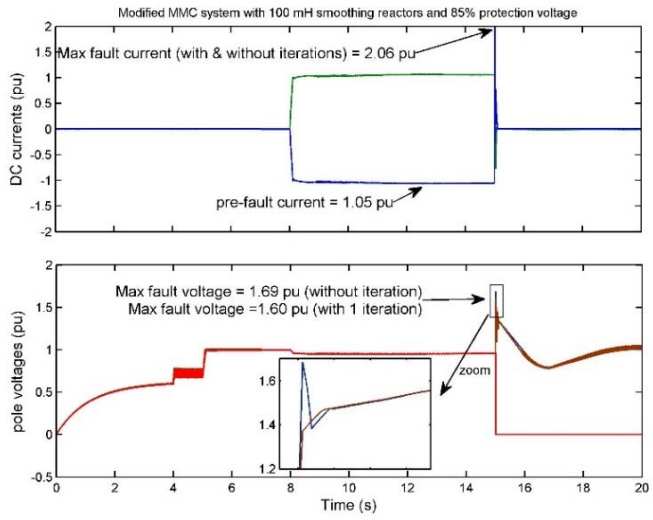


Fig. 8 Pole-to-ground fault on FS2 system; effect of iterations on peak voltage during fault

C. Zhoushan STATCOM-MMC

The ZS1 model runs on the same RT-LAB system as FS1/FS2: an OP5600 combined with an OP7020 for the MMC cells, all running in real-time.

In the test, we first bring the STATCOM model to its nominal working point, which is P=0 and Q=0. Then, we apply a pole-to ground fault, with no other actions after this fault on the part of the controls.

The resulting DC bus voltages are depicted in Fig. 9 and clearly show the effect of iterations on simulation accuracy. Indeed, without iterations, the healthy pole voltage has a spike at 1.935 PU (387 kV) while the same voltage peaks at 1.685 PU (337 kV) in the simulation **with** iterations (i.e. no voltage spike in the figure when iterations are activated).

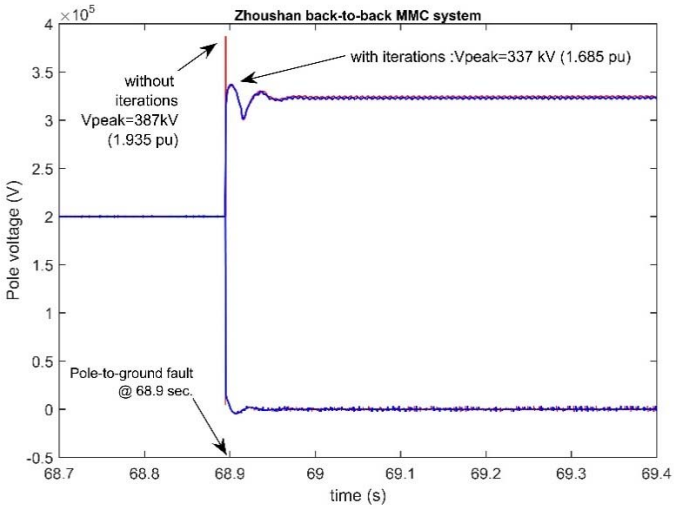


Fig. 9 DC bus voltages of ZS1 model during pole-to-ground fault

VIII. REAL-TIME PERFORMANCE

The three models and test cases presented in this paper, FS1, FS2 and ZS1, with iterations, run in hard real-time on the RT-LAB DRTS composed of one OP5600, using only 4 cores out of the 20 available and a Virtex-7 based OP7020 extension box. CPU time step is 25 µs. MMC model sample time and gate resolution on FPGA is 500 nanoseconds. No external I/Os were used during the tests but as the MMC I/Os are managed by the FPGA, I/O usage will not affect the DRTS performance.

In the case of the ZS1 model, further tests were made during commissioning and it was found that the CPU time step could be decreased down to 23 µs, with external controllers attached.

IX. CONCLUSION

This paper had two main objectives. The first was to demonstrate that a fully-detailed MMC link can be simulated in real-time using a combination of CPUs and FPGA. Two MMC configurations were studied: one derived from the France-Spain MMC-HVDC system: the models included two stations, each with fully-detailed 401-level MMC converters with 4800 half-bridge cells in total. A second case was also presented using a 271-level MMC station in STATCOM mode. Both models effectively run in the OPAL-RT DRTS at a time step of 25µs and with up to 4800 HBC of the MMC converters running of the Virtex-7 of the OP7020 FPGA extension.

The second objective of the paper was to demonstrate the real-time iteration capability of the SSN solver in a complex power system involving MMC converters. Two cases showed the importance of iterations in fault mode. The first case is a modified France-Spain link model with added 100 mH DC reactor and 85% of nominal MOV protection voltage; in this case there is a 0.09 PU pole voltage difference between iterated and non-iterated simulations involving a pole-to-ground fault. The second case is an MMC-HVDC station configured as a STATCOM device; in this case, there is 0.25 PU difference in pole voltage between iterated and non-iterated case involving a pole-to-ground fault.

In both cases, the iterated simulations clearly have a physically explainable behavior while the non-iterated one shows inaccuracy at the time of the fault. This should not come as a surprise because most general purpose algebraic-differential equation simulation tools are iterative by design. Non-iterative fixed-step solvers have been traditionally favored in real-time simulators, mainly for calculation speed reasons. The continuous advances in micro-processor technology over the last four decades is slowly changing this paradigm in favor of more common, iterative solvers.

REFERENCES

[1] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range,” Proc. Power Tech Conf., Bologna, Italy, 2003.

[2] H. Saad, S. Dennetiere, J. Mahseredjian, et al., "Modular Multilevel Converter Models for Electromagnetic Transients," , *IEEE Trans. on Power Delivery*, vol.29, no.3, pp.1481,1489, June 2014

[3] H. Saad, T. Ould-Bachir, J. Mahseredjian, C. Dufour, S. Dennetière, and S. Nguefeu “Real-time simulation of MMCs using CPU and FPGA”, *IEEE Trans. on Power Electronics*, vol.30, no.1, pp.259,267, Jan. 2015

[4] S. Dennetière, S. Nguefeu, H. Saad, J. Mahseredjian, "Modeling of Modular Multilevel Converters for the France-Spain link", *Proceedings of the International Conference on Power Systems Transients (IPST'13)*, Vancouver, Canada July 18-20, 2013

[5] S. Dennetière, H. Saad, B. Clerc, "Setup and performances of the real-time simulation platform connected to the INELFE control system", *Proceedings of the International Conference on Power Systems Transients (IPST'15)*, Cavtat, Croatia, June 15-18, 2015.

[6] O. Tremblay, M. Fecteau, P. Prud’homme, “Precise Algorithm for Nonlinear Elements in Large-Scale Real-Time Simulator,” Proc. of the 2012 CIGRÉ conference, Montréal, Qc, Canada, Sept. 24-26, 2013

[7] J. Hu, L. Yu, Z. Zhang, and J. Lu, “Research on the DC faults in multi-terminal DC transmission system based on MMC”, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 5, May 2013

[8] C. Dufour, J. Mahseredjian , J. Bélanger, “A Combined State-Space Nodal Method for the Simulation of Power System Transients”, *IEEE Trans. Power Delivery*, Vol. 26, no. 2, April 2011, pp. 928-935

[9] C. Dufour, O. Tremblay, “Iterative Algorithms of Surge Arrester for Real-Time Simulators”, *18th Power Systems Computation Conference (PSCC'14)*, Wroclaw, Poland, August 18-22, 2014

[10] J. Mahseredjian, S. Dennetière, L. Dubé, B. Khodabakhchian and L. Gérin-Lajoie: “On a new approach for the simulation of transients in power systems”. *Electric Power Systems Research*, Vol. 77, Issue 11, September 2007, pp. 1514-1520.

[11] C. Dufour, G. Sapienza, “Testing 750 Node Distribution Grids and Devices using Optimized Parallel Delay-Free Real-time Solvers and Modern Grid Protocols”, 2015 International Symposium on Smart Electric Distribution Systems and Technologies (EDST-15), Vienna, Austria, Sept. 8-11, 2015

[12] Wei Li, L-A Gregoire, J. Bélanger, “Control and Performance of a Modular Multilevel Converter System,” *in Proc. of CIGRE, Canada, Conf. on Power Systems*, Halifax, Sept., 2011.

[13] H. Saad, C. Dufour, J. Mahseredjian, S. Dennetière, S. Nguefeu, “Real Time simulation of MMCs using the State-Space Nodal Approach”, Proceedings of the IPST '13 conference - Vancouver, British Columbia, Canada, July 18-20, 2013

[14] T. Maguire, B. Warkentin, Y. Chen, J. Hasler, “Efficient Techniques for Real Time Simulation of MMC Systems”, Proceedings of the IPST '13 conference - Vancouver, British Columbia, Canada, July 18-20, 2013

[15] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, T. Jonsson “VSC-HVDC Transmission with Cascaded Two-Level Converters” Proceeding of CIGRE 2010 conference, Paris, France, August 2010.

[16] Wei Li, J. Bélanger, “An Equivalent Circuit Method for Modelling and Simulation of Modular Multilevel Converter in Real-time HIL Test Bench”, IEEE Transaction on Power Systems, 2016. (accepted)

[17] Gang Li, Yunlong Dong, Jie Tian ,Weihua Wang, Wei Li, J. Bélanger, “Factory Acceptance Test of a Five-terminal MMC Control and Protection System using Hardware-in-the-loop Method”, Proc. of 2015 IEEE Power & Energy Society General Meeting, Denver, USA, July 26-30, 2015

[18] Zhe Zhu, Xiaolin Li, Hong Rao, Weihua Wang and Wei Li, “Testing a complete control and protection system for multi-terminal MMC HVDC links using hardware-in-the-loop simulation”, IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, pp. 4402-4408

[19] Kaijian Ou, Hong Rao, Zexiang Cai, Haiping Guo, Xuehua Lin, Lin Guan, Trevor Maguire, Bruce Warkentin, and Yuan Chen, “MMC-HVDC Simulation and Testing Based on Real-Time Digital Simulator and Physical Control System”, IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol.2, No.4, Dec. 2014.