

OP5362 Foundation Fieldbus Mezzanine User Manual

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SYMBOL DEFINITIONS

The following table lists the symbols used in this document to denote certain conditions:

Symbol	Definition
Ċ	ATTENTION: Identifies information that requires special consideration
	TIP: Identifies advice or hints for the user, often in terms of performing a task
F	REFERENCE _ INTERNAL: Identifies an additional source of information within the bookset.
CAUTION	Indicates a situation which, if not avoided, may result in equipment or work (data) on the system being damaged or lost, or may result in the inability to properly operate the process.
	Indicates a situation where users must observe precautions for handling electrostatic sensitive devices.
	CAUTION: Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury. It may also be used to alert against unsafe practices.
	WARNING: Indicates a potentially hazardous situation which, if not avoided, could result in serious injury or death.

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OP5362 FOUNDATION FIELDBUS MEZZANINE

The OP5362 is a type B mezzanine designed to be installed on an OPAL-RT carrier board. It uses the Foundation Fieldbus communication system, which is available in two implementations. The OP5362 uses the H1 configuration, which operates at 31.25 kbit per second and provides communication over standard twisted-pair wiring.

The Digital In/Out (DIO) signals are connected to the FPGA via connector J2. The data are processed and formatted on-board to frame serialize and convert them to an H1 serial message.

REQUIREMENTS

SOFTWARE

- QNX or Redhat o/s
- RT-LAB 10.4.3 and higher

HARDWARE

- OP5600 HIL simulator
- OP5600 I/O Expansion Unit:

FEATURES

- User selectable mode, either regular Transmit/Receive or Loopback
- User selectable DGND and AGND connection
- LED transmit/receive status indicators
- LED power source indicators
- Output transformer for H1 connection compatibility.

INSTALLATION AND CONFIGURATION

The OP5362 Foundation Fieldbus mezzanine must be inserted into the OPAL-RT carrier board using great care. Two polarized connectors fasten the module in the suitable position and four screws affix it for a more secure connection to the carrier.

Make sure that the connectors are properly aligned; they should fit together easily. Use light pressure to push the OP5362 board into the carrier board.

The OP5362 module can only be used with an OPAL-RT's carrier board. Its identification on the carrier board is determined by the FPGA controller bitstream.



CIRCUIT LAYOUT DIAGRAMS

When the OP5362 is installed on the carrier board, only the top of the circuit board is visible, as shown in Figure 1. The connectors are located on the bottom of the board (see Figure 2) and fit snugly into the connectors on the carrier board.

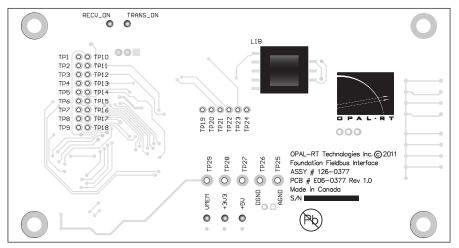
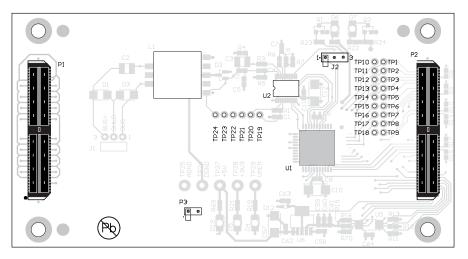


Figure 1: OP5362 analog to digital converter module (top view)





Carrier board connector

Board Components

The OP5362 board contains certain components that are essential to using the Foundation Fieldbus with the FPGA. These components require no interaction but their function is:

Position on board	Description	
U1:	Controller is to address and to frame the data in a H1 type parallel data stream	
U2 :	Transceiver is to convert the parallel byte stream in a serial data stream.	
L1B:	Transformer, and its associated circuit, is to convert the serial data in a floating isolated current link compatible with the H1 standard.	

Board Interfaces

The board has interfaces that let the user select from predetermined functions or that display statuses for board operation:

Position on board	Description
J2 :	3-pin jumper determines the connection type for the FPGA connection, whether the DIO signals will be in Loopback mode or in regular Transmit/Receive mode. See Figure 3 for details on jumper positions.
P3 :	2-pin jumper determines whether the DGND and AGND are connected. See Figure 3 for details on jumper positions.
RECV_ON	Indicates whether the board is receiving data.
TRANS_ON:	Indicates whether the board is transmitting data.
VMEM:	Indicates that the on-board EEPROM identifier is connected to a power source.
+3.3V	Indicates that the 3.3 V power is active.
+5V:	Indicates that the 5 V power is active.

The diagram provides a visual explanation of jumper position settings.

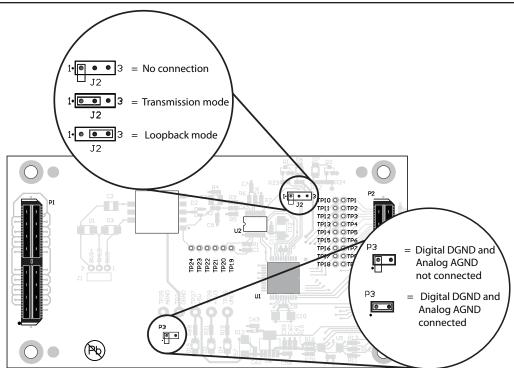


Figure 3: jumper position diagram

SCHEMATIC

The first stage, Controller, gets data from the FPGA and frames it in an H1 parallel data stream.

The second stage, Transceiver, converts the parallel data stream to a serial data stream.

The third stage, Transformer, converts the TTL data stream to a floating isolated current link compatible with the H1 standard.

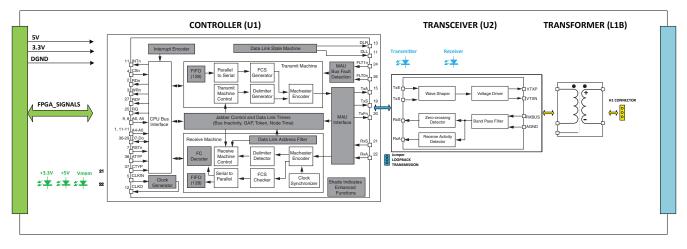


Figure 4: OP5362 schematic

SPECIFICATIONS

Product name	OP5362 Foundation Fieldbus mezzanine
Part number	126-0377
Power	3.3 V @ 100 mA 5V @ 100 mA
Connectivity	H1 compatible
Certification and standards	IEC 61804."3
Dimensions	6.60 cm x 12.50 cm (2.6" x 4.92")
Operating temperature	10 to 40 °C (50 to 104°F)
Storage temperature	-55 to 85°C (-67 to 185°F)
Relative humidity	10 to 90%, non condensing
Maximum altitude	2,000 m (6562 ft.)

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