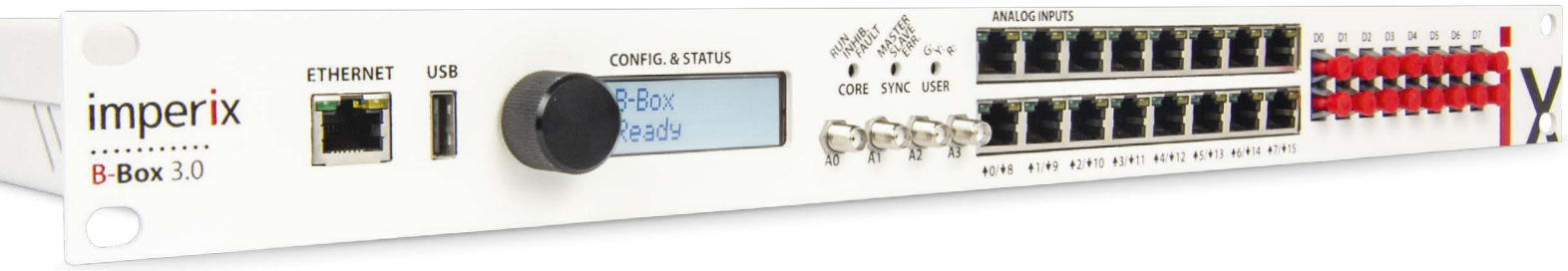
B-Box RCP 3.0

Rapid prototyping controller

The B-Box RCP accelerates the development and experimental validation of converter control techniques in a laboratory environment.



GENERAL DESCRIPTION

B-Box RCP is a modular control platform, exclusively tailored for Rapid Control Prototyping (RCP) applications in power electronics. Thanks to its high performance and flexibility, it facilitates the experimental validation of power converters control techniques in R&D environments.

The B-Box notably distinguishes from other RCP solutions by its fully programmable analog front-end, its advanced Pulse-Width Modulation (PWM) capabilities, as well as its numerous and specialized I/Os.

Also, this system has been designed from the start with synchronous sampling applications in mind. It therefore offers a large configurability and guarantees a very strict management of timings and phase shifts, from analog inputs to PWM outputs, including in networked configurations.

Performance is not left on the side either, since its dual-core ARM processor and Kintex-grade FPGA support closed loop control application up to hundreds of kHz! Besides, for the most demanding applications, B-Boxes can be stacked up forming a networked control system of up to 64 units and thousands of I/Os.

Networked B-Box configurations are supported by *RealSync*, a proprietary technology that guarantees sub-µs transfer latency and ns-scale synchronization accuracy. Thanks to this technology, stacked configurations can be used in a totally transparent fashion, as if all FPGA resources and I/Os belonged to one single controller.

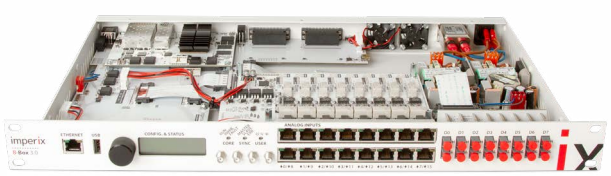
TYPICAL APPLICATIONS

Thanks to its high flexibility, practically any power electronic application can be ideally addressed with B-Box RCP, ranging from grid-tied appliances to electric drives, energy storage systems, renewables, electric mobility, etc.

That said, B-Box RCP is most attractive in demanding applications, either in terms of I/O count (e.g. multilevel converters), in terms of performance or even both. Notably, systems based on wide band gap devices such as SiC or GaN often simultaneously require high-precision PWM generation as well as a fast closed-loop control speed.

KEY FEATURES AND SPECIFICATIONS

- Stackable up to 64 units
- Dual-core 1 GHz ARM processor
- Kintex-grade FPGA (user programmable)
- Software-independent protections
- Programmable analog front-end
- Up to 250 kHz closed loop control frequency
- 134 user I/Os per unit
- Advanced pulse-width modulators (PWM)



FRONT PANEL

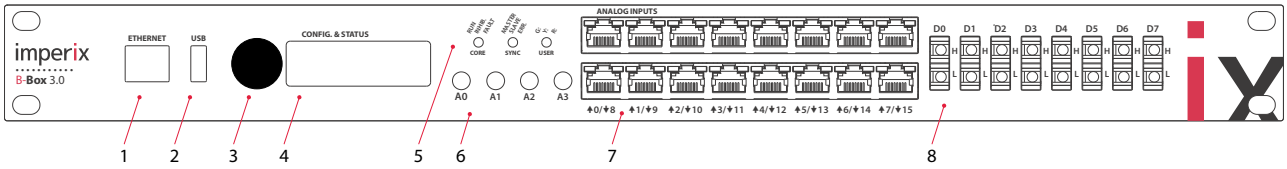


Fig. 1. Front panel view of the B-Box RCP.

1) Gigabit Ethernet port (RJ45)
2) Front panel USB port
3) Rotary and push button
4) LCD screen
5) System and user LEDs
6) Analog outputs (SMA, ±5V)
7) Analog inputs (RJ45, ±10V)
8) Optical PWM outputs (PWM lanes #0-#15)

BACK PANEL

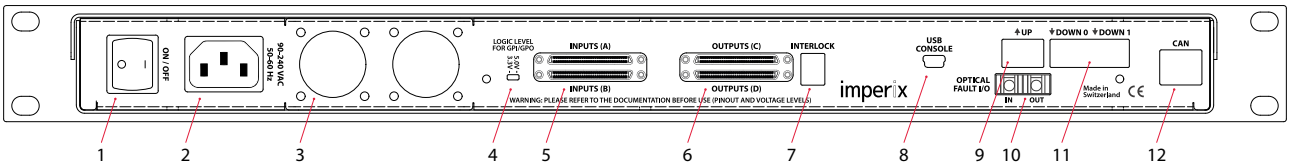


Fig. 2. Back panel view of the B-Box RCP.

1) AC mains switch (ON/OFF)
2) AC mains socket (IEC C14, 110-230V)
3) Fan outlets
4) Selector for GPI/GPO voltage (3.3V or 5.0V)
5) Digital inputs – Connectors A and B (VHDCI HD68)
6) Digital outputs – Connectors C and D (VHDCI HD68)
7) Electrical interlock connector (IN/OUT)
8) Console port (system debug)
9) SFP interconnect – UP link
10) Optical interlock (IN/OUT)
11) SFP interconnect – DOWN links
12) CAN socket (RJ45)

DEVICE CONTENT

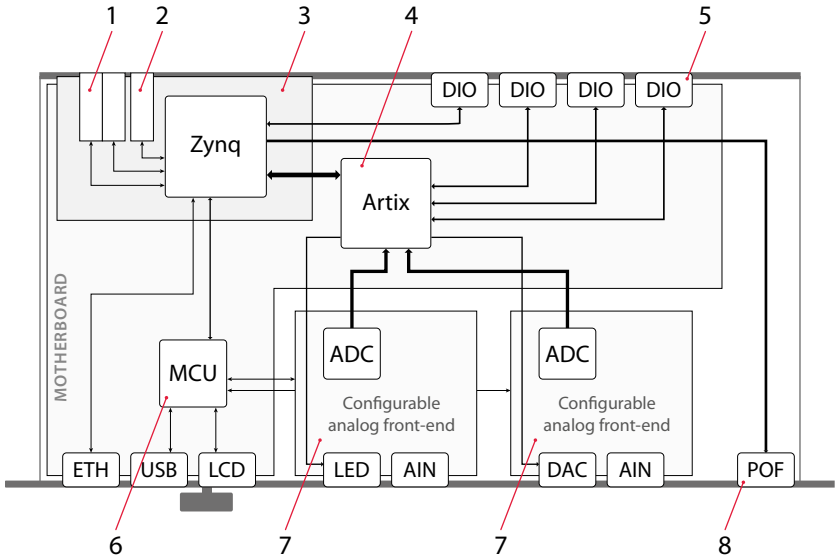
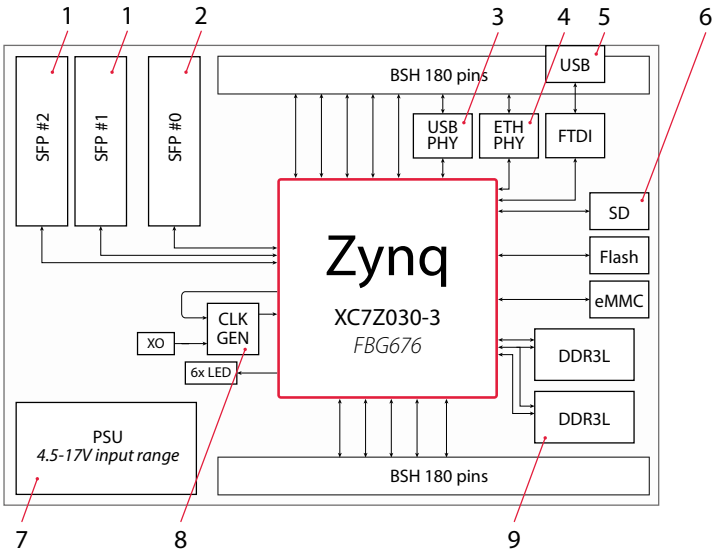


Fig. 3. Simplified system description of the B-Box RCP.

1) SFP Interconnect – DOWN links
2) SFP Interconnect – UP link
3) B-Board processing module
4) Auxiliary FPGA
5) Digital inputs & outputs
6) Frontpanel micro controller
7) Analog front-end board(s)
8) Plastic Optical Fiber (POF) output module

B-BOARD PROCESSING MODULE DESCRIPTION

1) SFP Interconnect – DOWN links
2) SFP Interconnect – UP link
3) USB OTG (on bottom BSH)
4) Gigabit Ethernet (on bottom BSH)
5) Console port



6) Onboard memories:
   – SD card slot
   – 32 MB Flash (program)
   – 8 GB Flash (logging)
7) Wide input range on-board power supply
8) SFP clocks management
9) DDR memory (1 GB)

Fig. 4. Simplified structure of the B-Board processing module.

MAIN SPECIFICATIONS

Component	Specification	Component	Specification
System on chip	*Xilinx Zynq XC7Z030-3FBG676E Speed grade -3*	*PWM outputs*	*Various modulators 4 ns resolution*
Processing system	*ARM Cortex A9 1 Ghz x2 1GB DDR3*		*Optical 50 Mbps x16 Electrical (3V3) x32*
Programmable logic (FPGA)	*Kintex 7 125K Artix 7 35T (auxiliary)*	*Analog inputs*	*16 bits / 500ksps (simultaneous) x16 Fully configurable front-end*
Storage	*Flash 16MB x2 micro SD + eMMC 8GB*	*General-purpose digital outputs (GPO)*	*Electrical (3.3V/5.0V) x16*
		General-purpose digital inputs (GPI)	*Electrical (3.3V/5.0V) x16*
Communication	*USB 2.0 high speed (type A) x1 USB console x1*	*Incremental decoder inputs*	*3-pins (A,B,Z) x4 Shared with GPI inputs*
	Ethernet 1Gbps (RJ45) x1	*User High-speed I/Os*	*FPGA direct (3V3) x36*
	SFP+ 5Gbps x3	*Fault inputs / outputs*	*Digital (3V3) x16 Optical interlock x1 Electrical interlock (5.0V) x1*

Table 1. Main system specifications for B-Box RCP.

MAXIMUM I/O CAPABILITIES

Component	Characteristics	Single (1 unit)	Stacked (64 units)
Analog inputs	*Fully configurable (gain, impedance, filter, protection)*	*16*	*1024*
PWM outputs	*Optical, 50 Mbps*	*16*	*1024*
	Electrical, >500 Mbps	*32*	*2048*
General-purpose digital outputs (GPO)	*Electrical, >100 Mbps*	*16*	*1024*
General-purpose digital inputs (GPI)	*Electrical, >100 Mbps*	*16*	*1024*

Table 2. Maximum I/O count per B-Box RCP unit and in networked configuration.

LOGICAL STRUCTURE

The B-Box RCP operates thanks to an association between two CPU core and dedicated peripherals implemented in programmable logic. The distribution of tasks is as follows:

- CPU0: Running on Linux, the first core is responsible for loading the application code, supervising the system execution and managing the data logging.
- CPU1: Running on BBOS (lightweight secured proprietary operating system), the second core executes the application-level control code developed by the user.
- FPGA: The programmable logic area contains all the application-specific peripherals. By default, the corresponding firmware is fixed.

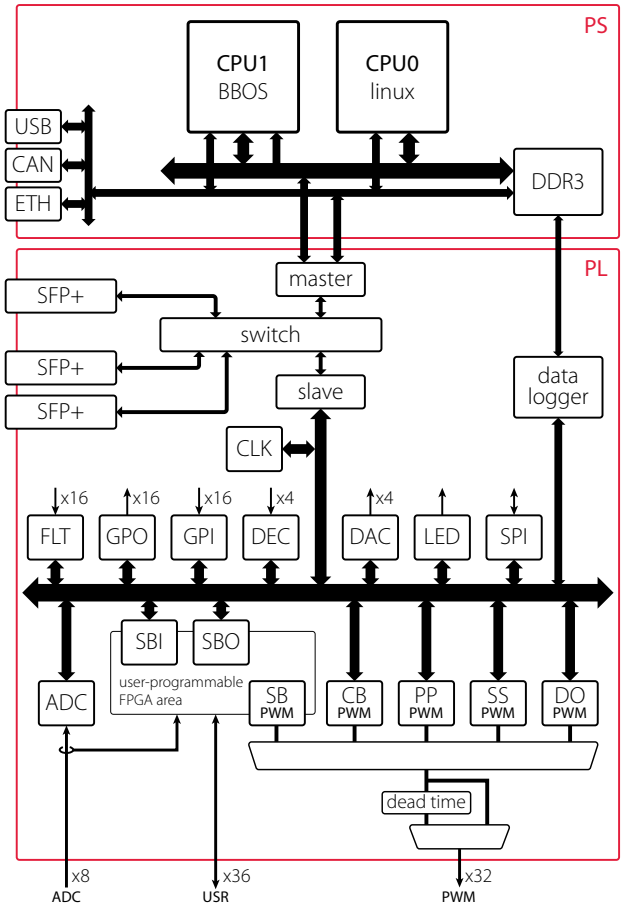


Fig. 5. Functional overview of the B-Box control platform.

The pre-implemented FPGA peripherals are as follows:

- CLK: Offers clock generators with up to four separate time-bases that can be used with other peripherals.
- ADC: Acquires data from the 16 analog input channels located on the analog front end.
- DAC: Updates the 4 analog output channels (SMA connectors on the front side of the device).
- SBI: Provides easy-to-use access for inbound data traffic from the user-programmable area (sandbox).
- SBO: Provides easy-to-use access for outbound data traffic from the user-programmable area (sandbox).
- CB-PWM: Contains 32 fully-configurable carrier-based modulators (conventional sampled PWM).
- SS-PWM: Implements multilevel modulation for modular converters using a Sort-&-Select voltage balancing technique such as commonly used in Modular Multilevel Converters (MMC). It achieves the balancing of floating capacitors, while maximizing the ration between waveform performance and average switching frequency.
- PP-PWM: Provides hardware support for the generation of Programmed Patterns. It is useful for PWM techniques such as Selective Harmonic Elimination (SHE) or Optimized Pulse Patterns (OPP) in general.
- DO-PWM: Offers a Direct Output operation, allowing to force a specific lane state (0 or 1). This is useful for control techniques such as Model Predictive Control (MPC) or Direct Torque Control (DTC).
- SB-PWM: Provides access to the PWM outputs from the user-programmable area (sandbox).
- GPO: Offers 16 General-Purpose Outputs.
- GPI: Offers 16 General-Purpose Inputs.
- FLT: Offers 16 configurable fault inputs. These inputs can also be used as general-purpose inputs.
- LED: Drives the 3 LEDs available on the front panel.
- DEC: Support the decoding of signals produced by up to four incremental encoders for motor drive applications.
- ETH: Supports data exchanges on Ethernet (TCP/UDP).
- CAN: Provides connectivity with CAN peripherals.
- SPI: Provides SPI connectivity (bidirectional).

ANALOG INPUTS

The B-Box RCP features a fully programmable analog front-end with 16 inputs channels as in Fig. 6. The overall performance specifications are indicated in Table 3. Further analog–to–digital performance specifications are given in Table 7.

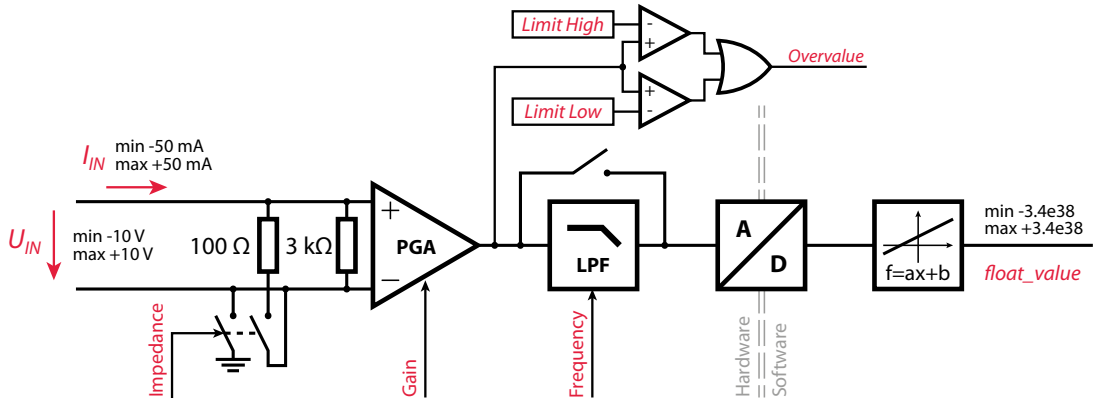


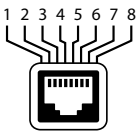
Fig. 6. Block diagram of each channel of the analog input front-end.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage range	Differential mode		±10.0		V
	Common mode		±11.2		V
Absolute maximum tolerable input voltage	On any pin		±56		V
Input impedance	High Z mode / full differential input	2.99	3	3.01	kΩ
			2.2		nF
	Low Z mode / single ended input	99	100	101	Ω
			2.2		nF
Large signal bandwidth	-3 dB, without any filter	400	410		kHz
CMRR (differential input mode only)	G = 2, 0 Hz – 400 kHz	> 65	> 72		dB
	G = 2, 1.5Mhz	> 41	> 46		dB
	G = 2, > 10 Mhz	> 69	> 74		dB
Total gain error (uncalibrated)	DC, 3 kΩ differential input mode		±0.8	±1.5	%
	DC, 100 Ω single-ended input mode		±1.4	±1.8	%
Gain stability	0 - 85°C		±0.12	±0.21	%
Offset (uncalibrated)	G = 1, without filter (other gains are better)		±3.6	±15.3	LSB
	G = 1, with filter ON	+16.4	+20.1	+23.6	LSB
Offset stability	0 – 85°C, without filter		±2.1	±4.3	LSB
	0 – 85°C, with filter ON		±5.3	±9.3	LSB
Embedded power supply voltage	$I_{OUT} < I_{OUT,max}$ (output protection not triggered)	±14.6	±15.0	±15.4	V
Embedded power supply output current	per channel			150	mA
	all channels			1.5	A

Table 3. Overall performance specifications of the analog front-end (each channel).

ANALOG INPUT CONNECTORS

Analog inputs rely on RJ45 connectors. This allows the use of well shielded twisted pair cables for the connection to sensors, with a good EMI performance.



Pin	Pair	Color	Description
1	2	orange stripe	+15 V
2	2	orange solid	+15 V
3	3	green stripe	0 V
4	1	blue solid	Positive input / current input
5	1	blue stripe	Negative input / ground
6	3	green solid	0 V
7	4	brown stripe	-15 V
8	4	brown solid	-15 V

Table 4. Pinout of the analog inputs.

SELECTABLE INPUT IMPEDANCE

For each channel, the input impedance can be selected so as to implement one of the following configurations:

» High impendance mode: 3 kΩ, full differential mode. This is the default configuration, which is mostly useful when the acquired quantity is a voltage proportional to the measurement.

» Low impedance mode: 100 Ω, single-ended signalling. This is typically useful when the acquired quantity is a current proportional to the measurement.

PROGRAMMABLE-GAIN AMPLIFIER

Each channel features a AD8251 programmable gain amplifier (PGA) from Analog Devices. The selection of a particular gain typically allows to maximize the ADC input range, notably improving the resolution on the measured value. The possible gain configurations are G = 1, G = 2, G = 4 or G = 8.

PROGRAMMABLE LOW-PASS FILTER (WITH BYPASS)

Each channel features a LTC1065 programmable low-pass filter from Linear Technology with the possible cut-off frequencies given in Table 5. The filter is a 5th-order Bessel filter, hence with a practically flat group delay. Attenuation is 80 dB at 8 times the cut-off frequency.

The filter is controlled by a variable-frequency clock that is generated by a local microcontroller. As such, the cut-off frequency can be easily and directly selected from the front panel of the B-Box.

When not used, the filter is physically bypassed by a controllable relay for superior noise and offset performance. When used, the offset of each channel should be properly calibrated with the selected cut-off frequency (as this is indeed a parameter that may significatively vary from part-to-part).

Cut-off frequency	Group delay	Cut-off frequency	Group delay
Filter OFF	*0.0 µs*		
0.5 kHz	*800 µs*	*8.0 kHz*	*50 µs*
1.0 kHz	*400 µs*	*10 kHz*	*40 µs*
1.6 kHz	*250 µs*	*16 kHz*	*25 µs*
2.5 kHz	*160 µs*	*20 kHz*	*20 µs*
4.0 kHz	*100 µs*	*32 kHz*	*12.5 µs*
6.4 kHz	*62.5 µs*	*40 kHz*	*10 µs*

Table 5. Possible low-pass filter (LPF) configurations.

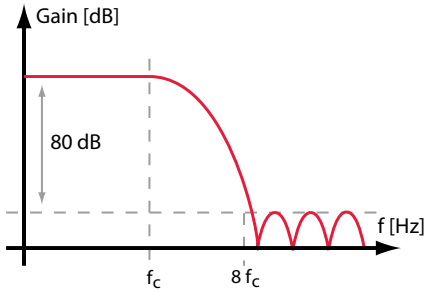


Fig. 7. Frequency response of the low-pass filter.

PROTECTION THRESHOLDS

Each channel features two programmable analog comparators, which can be set to define low and high input voltage thresholds. When either of these thresholds is crossed, the PWM signals (optical and electrical) are instantly blocked and the B-Box set to FAULT state.

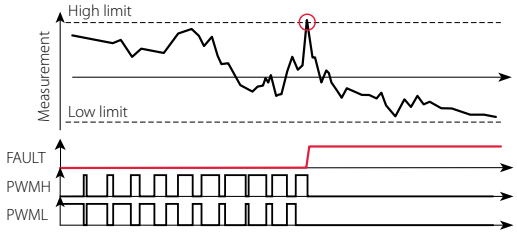


Fig. 8. Operating principle of the protection thresholds.

Characteristic	Min.	Typ.	Max.	Unit
Configurable range		*±10.0*		*V*
Setting resolution		*0,1*		*V*
Setting accuracy	*± 10 % m.v. ± 100 mV*			
Response delay to blocking of PWM signals		*1.4*	*1.6*	*µs*

Table 6. Performance specifications of the programmable thresholds.

ANALOG-TO-DIGITAL CONVERTER

A-to-D conversion is achieved with two ADS8568 from TI. The devices guarantee simultaneous sampling on all channels. The sampling clock is freely selectable amount all four CLK sources (see corresponding section on page 11).

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Resolution			*16*		*bits*
Noise floor	*G = 1, differential input mode, no filter*		*0.8*	*1.7*	*LSB (rms)*
Sampling rate		*0.001*		*500*	*ksps*
Sampling jitter	*Same B-Box*		*± 2.1*		*ns*
	Across all B-Boxes		*± 3.6*		*ns*
Conversion time	*All channels*			*1.98*	*µs*
Data transfer delay		*See Fig. 9.*			*ns*

Table 7. Performance specifications of the A/D conversion.

Data retrieval from A/D converters to the processing cores is achieved through FPGA logic and over the RealSync network in case of multi-Bbox operation. Transfer delays vary with the amount of data to be transferred (see Fig. 9). The overall delay from sampling to cache memory is therefore the sum of the ADC conversion time and data transfer delay.

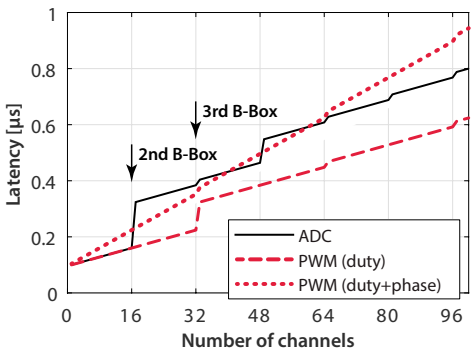


Fig. 9. Data transfert delay as a function of the number of channels.

OPTICAL OUTPUTS

PWM lanes #0 to #15 are available on optical fiber outputs. They make use of FT50MHNR transmitters from Firecomms.[1] By default, two consecutive PWM lanes are associated to form a PWM channel. Several configurations of PWM channels are possible, similarly to electrical PWM outputs:

- PWMH + PWML: high- and low-side gate drive signals, i.e. pseudo-complimentary signals with a configurable dead time between their '1' states. In this case two PWM lanes form a PWM channel.
- PWM + ACTIVE: PWM and switching authorization signals, i.e. one switching signal and one for blocking / unblocking the operation. In this case, two PWM lanes also form a PWM channel.
- INDEPENDENT: each PWM lane is linked to its own PWM modulator. In this case, no PWM channel is formed and dead time is not enforced.

In pseudo-complimentary operation (PWMH + PWML), a dead time can be freely configured by software.

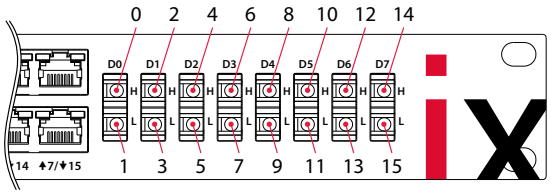


Fig. 10. Physical assignment of PWM lanes.

The overall timing accuracy of the optical outputs is shown in Table 8. These specifications encompass all sources of timing uncertainly up to the optical signals, including the B-Box–to–B-Box synchronization accuracy for networked configurations. Additional details regarding synchronization are given in the section addressing clock generation (page 11).

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Wavelength		*640*	*650*	*670*	*nm*
Propagation delay asymmetry	*Any two signals, same B-Box, 3σ*			*± 13*	*ns*
	Any two signals, across all networked B-Boxes, 3σ			*± 15*	*ns*
Relative jitter (optic)	*Any two signals, same B-Box, 3σ*			*± 1.8*	*ns*
	Any two signals across all networked B-Boxes, 3σ			*± 2.1*	*ns*

Table 8. Performance specifications of the optical PWM outputs.

ANALOG OUTPUTS

The B-Box RCP features 4 analog output channels, available through the 4 SMA connectors present on its front panel. DAC data are updated continuously and successively channel-by-channel.

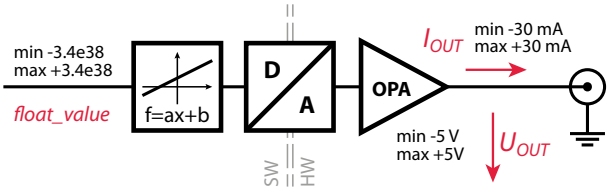


Fig. 11. Block diagram of each channel of the analog output front-end.

Characteristic	Min.	Typ.	Max.	Unit
Resolution		*16*		*bits*
Output voltage range		*± 5.0*		*V*
Maximum tolerable output current	*± 15*	*± 30*		*mA*
Gain error		*± 1.1*		*%*
Offset		*± 0.2*		*mV*
Settling time		*6.5*		*µs*

Table 9. Performance specifications of the analog outputs.

1 All PWM lanes are also available on the 3.3V electrical outputs on the rear side of the device.

DIGITAL INPUTS

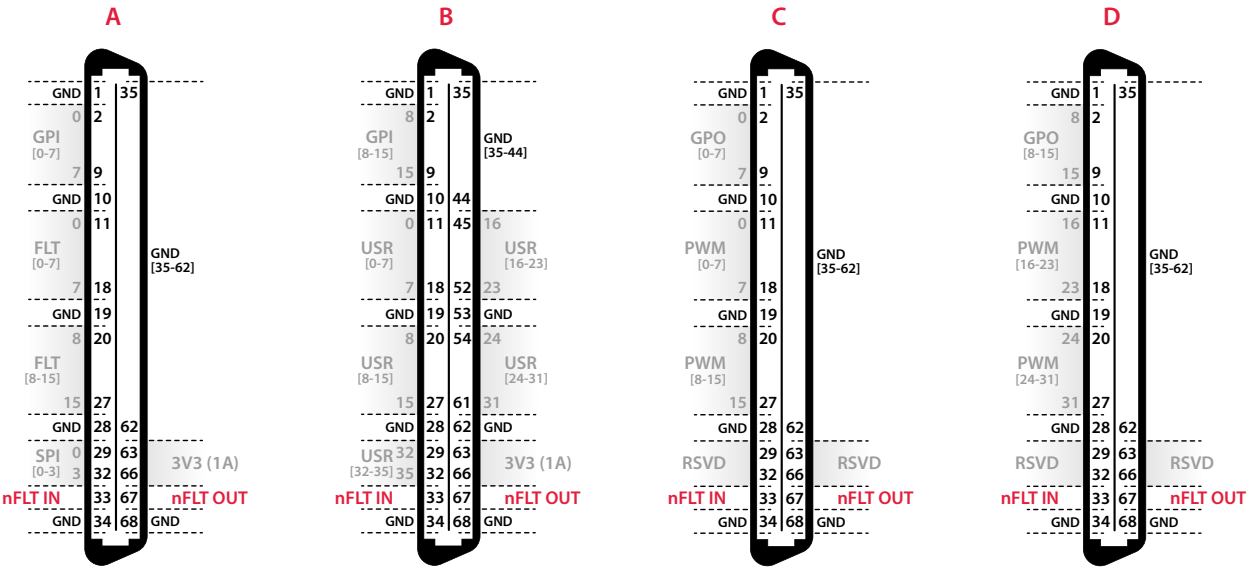
The electrical digital inputs are grouped on the (A) and (B) high-speed connectors (part number : Molex 0743371054). The following functions are available :

» GPI : General purpose inputs (16 bits)
» FLT : Fault feedback inputs (16 bits)
» SPI : Multi-function acquisition bus (4 bits)
» USR : Fully-configurable input / output bus (32+4 bits)

DIGITAL OUTPUTS

The electrical digital outputs are grouped on the (C) and (D) connectors (part number : Molex 0743371054). The following functions are available :

» GPO : General purpose outputs (16 bits)
» PWM : Pulse-width modulated signals (32 bits)



Pins	Signal	Level
1, 10, 19, 28, 34, 35-62, 68	*GND*	
2-9	*GPI 0-7*	*3.3/5V*
11-18	*FLT 0-7*	*3.3V*
20-27	*FLT 8-15*	*3.3V*
29-32	*SPI 0-3*	*3.3V*
63-66	*3V3*	
33	*Fault IN*	*3.3V*
67	*Fault OUT*	*3.3V*

INPUTS (A)

Pins	Signal	Level
1, 10, 19, 28, 34, 35-44, 53, 62, 68	*GND*	
2-9	*GPI 8-15*	*3.3/5V*
11-18, 20-27	*USR 0-15*	*3.3V*
45-52, 54-61	*USR 16-31*	*3.3V*
29-32	*USR 32-35*	*3.3V*
63-66	*3V3*	
33	*Fault IN*	*3.3V*
67	*Fault OUT*	*3.3V*

INPUTS (B)

Table 10. Pinout of the digital inputs (A) and (B).

Pins	Signal	Level
1, 10, 19, 28, 34, 35-62, 68	*GND*	
2-9	*GPO 0-7*	*3.3/5V*
11-18	*PWM 0-7*	*3.3V*
20-27	*PWM 8-15*	*3.3V*
29-32, 63-66	*RSVD*	
33	*Fault IN*	*3.3V*
67	*Fault OUT*	*3.3V*

OUTPUTS (C)

Pins	Signal	Level
1, 10, 19, 28, 34, 35-62, 68	*GND*	
2-9	*GPO 8-15*	*3.3/5V*
11-18	*PWM 16-23*	*3.3V*
20-27	*PWM 24-31*	*3.3V*
29-32, 63-66	*RSVD*	
33	*Fault IN*	*3.3V*
67	*Fault OUT*	*3.3V*

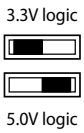
OUTPUTS (D)

Table 11. Pinout of the digital outputs (C) and (D).

Peripheral	Bit lanes	Level	Main functions and bus width	Alternate function	Connector	Internal topology	Typ. speed
GPI	*GPI 0-7*	*3.3 / 5 V*	*General-purpose inputs (16 bits)*	*Incremental decoder*	*A*	*Level shifted to 3.3 V*	*150 Mbps*
	GPI 8-15	*3.3 / 5 V*		*Incremental decoder*	*B*	*Double level shifted to 1.8 V*	*100 Mbps*
GPO	*GPO 0-7*	*3.3 / 5 V*	*General-purpose outputs (16 bits)*		*C*	*Level shifted from 3.3 V*	*150 Mbps*
	GPO 8-15	*3.3 / 5 V*			*D*	*Double level shifted from 1.8 V*	*100 Mbps*
PWM	*PWM 0-15*	*3.3 V*	*Pulse-width modulated signals (32 bits)*	*High-speed DOUT*	*C*	*Direct to Zynq*	*400 Mbps*
	PWM 16-31	*3.3 V*		*High-speed DOUT*	*D*	*Level shifted to 1.8V by Artix 7*	*250 Mbps*
FLT	*FLT 0-15*	*3.3 V*	*Fault feedback signals (16 bits)*	*High-speed DIN*	*A*	*Level shifted to 1.8V by Artix 7*	*250 Mbps*
SPI	*SPI 0-4*	*3.3 V*			*A*	*Level shifted to 1.8V by Artix 7*	
USR	*USR 0-35*	*3.3 V*			*B*	*Direct to Zynq*	*400 Mbps*

Table 12. General specifications of the digital signals available on the high-speed connectors.

WARNING:
Always make sure to apply and use the **appropriate voltage level** on each signal. Unexpected behavior or damages may occur in case of inappropriate voltage. The operating logic voltage can be easily selected using the corresponding switch on the rear side of the B-Box RCP unit. **This only applies to GPI and GPO.**



GENERAL-PURPOSE INPUTS (GPI) AND INCREMENTAL DECODER INPUTS (DEC)

16 inputs are available on connectors (A) and (B). These inputs are statically tied to the GPI block. The logic level can be selected to be 3.3 V or 5.0 V. The same inputs can also be used as incremental decoder inputs for the DEC peripheral.

Characteristic	Test conditions	Value	Unit
Maximum tolerable input voltage	*5.0 V*	*5.5*	*V*
	3.3 V	*3.6*	*V*
Propagation delay asymmetry	*Any two signals on same B-Box*	*< 5.0*	*ns*
	Any two signals across all B-Boxes	*< 7.0*	*ns*

Table 13. Performance specifications of the GPI/DEC inputs.

Pin	GPI signal	DEC signal	Pin	GPI signal	DEC signal
A2	*GPI 0*	*A0*	*B2*	*GPI 8*	*A2*
A3	*GPI 1*	*B0*	*B3*	*GPI 9*	*B2*
A4	*GPI 2*	*Z0*	*B4*	*GPI 10*	*Z2*
A5	*GPI 3*	*A1 or $\overline{A0}$*	*B5*	*GPI 11*	*A3 or $\overline{A2}$*
A6	*GPI 4*	*B1 or $\overline{B0}$*	*B6*	*GPI 12*	*B3 or $\overline{B2}$*
A7	*GPI 5*	*Z1 or $\overline{Z0}$*	*B7*	*GPI 13*	*Z3 or $\overline{Z2}$*
A8	*GPI 6*	*N/A*	*B8*	*GPI 14*	*N/A*
A9	*GPI 7*	*N/A*	*B9*	*GPI 15*	*N/A*

Table 14. Signal assignment for the GPI/DEC inputs.

GENERAL-PURPOSE OUTPUTS (GPO)

16 outputs are available, grouped into 2x8 pins on connectors (C) and (D). They are statically tied to the GPO block. The logic level can be freely selected to be 3.3 V or 5.0 V.

Characteristic	Test conditions	Value	Unit
Max. rise / fall time	*5.0 V*	*5*	*ns*
	3.3 V	*5*	*ns*
Propagation delay asymmetry	*Any two signals, on same B-Box*	*2.5*	*ns*
	Any two signals across all B-Boxes	*2.5*	*ns*
Current drive capability	*5.0 V*	*±32*	*mA*
	3.3 V	*±24*	*mA*

Table 15. Performance specifications of the GPO outputs.

FAULT FEEDBACK INPUTS (FLT)

16 digital input lanes are available as fault feedback signals. They can also be accessed as digital inputs. In case an external interface circuit is needed, some power can be drawn out of the 3.3 V pins (up to 1A typically).

Characteristic	Min.	Typ.	Max.	Unit
Response delay to blocking of PWM signals		*50*	*60*	*ns*
Operating voltage	*3.0*	*3.3*	*3.6*	*V*

Table 16. Performance specifications of the fault feedback inputs.

MULTI-FUNCTION ACQUISITION BUS (SPI)

A multi-purpose Serial Peripheral Interface (SPI) bus is available on connector (A). It is statically tied to the SPI block.

Characteristic	Min.	Typ.	Max.	Unit
Configurable clock frequency			*30*	*MHz*
Operating voltage	*3.0*	*3.3*	*3.6*	*V*

Table 17. Performance specifications of the SPI bus.

Pin	Name	Direction	Function description
A 29	*SCLK*	*Output*	*Data sampling clock*
A 30	*CS*	*Output*	*Chip select strobe*
A 31	*MISO*	*Input*	*Master In Slave Out data*
A 32	*MOSI*	*Output*	*Master Out Slave In data*

Table 18. Signal assignment of the SPI bus.

USER-CONFIGURABLE I/O BUS (USR)

The B-Box RCP features a high-speed bus of 36x bidirectional I/Os that is directly accessible from the user-programmable area (inside the Zynq chip). This area, also designated as sandbox offers easy-to-use access from / to the processing cores through the dedicated SBI and SBO blocks.

Characteristic	Min.	Typ.	Max.	Unit
Operating data bitrate (all lanes)			*400*	*Mbps*
Operating voltage	*3.0*	*3.3*	*3.6*	*V*

Table 19. Performance specifications of the USR bus.

Pin	Name	Direction	Function description
B 11-B 18	*USR 0-7*	*I/O*	*Any (e.g. data / address)*
B 20-B 27	*USR 8-15*	*I/O*	*Any (e.g. data / address)*
B 45-B 52	*USR 16-23*	*I/O*	*Any (e.g. data / address)*
B 54-B 61	*USR 24-31*	*I/O*	*Any (e.g. data / address)*
B 29-B 32	*USR 32-35*	*I/O*	*Any (e.g. data / address / strobes)*

Table 20. Signal assignment of the USR bus.

ELECTRICAL PWM OUTPUTS (PWM)

32 PWM lanes are available on connectors (C) and (D). The first 16 lanes (i.e. #0-15) are shared with optical outputs. Two consecutive PWM lanes are by default associated to form a PWM channel with three possible configurations:

- PWMH + PWML: high- and low-side signals with configurable dead time between their '1' states.
- PWM + ACTIVE: PWM and switching authorization signals, i.e. one switching signal and one for blocking / unblocking the operation.
- INDEPENDENT: each PWM lane is linked to its own PWM modulator. No dead time is enforced.

Table 21 summarizes the timing performance specifications.

Characteristic	Channels	Test conditions	Min.	Typ.	Max.	Unit
Propagation delay asymmetry	*PWM 0-15*	*Any two signals on same B-Box*			*± 1.6*	*ns*
	PWM 16-31				*± 2.3*	*ns*
	Any	*Any two signals on same B-Box*			*± 3.8*	*ns*
		Any two signals across all networked B-Boxes			*± 5.8*	*ns*
Relative jitter	*Any*	*Any two signals on same B-Box*			*± 0.4*	*ns*
		Any two signals across all networked B-Boxes			*± 0.7*	*ns*

Table 21. Performance specifications of the 3.3V electrical PWM outputs.

FAULT INTER-LOCKING SIGNALS

Fault inter-locking allows to coordinate emergency mechanisms between a B-Box RCP and other appliances, or across several B-Boxes or systems. These mechanisms are bi-directional as they can inform other devices about an internal fault condition or reciprocally receive external trigger signals. In a stacked configuration with multiple networked B-Boxes, fault inter-locking is intrinsically available thanks to the imperix *RealSync* protocol (optical fiber links).[1] Two types of inter-locking mechanisms are available on B-Box RCP:

- Electrical inter-lock: Labeled **INTERLOCK** on the rear side of the device. The connector is part number 1786837 from Phoenix Contact. The mating part is 1790108.
- Optical inter-lock: Labeled **OPTICAL FAULT I/O**. The optical interlock uses standard plastic optical fibers (POF) similar to the Avago HFBR family. The light is ON when no fault condition is active.

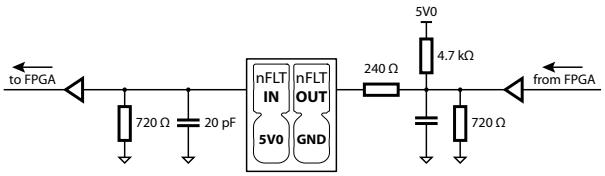


Fig. 12. Electrical circuit for the electrical inter-locking mechanism.

Characteristic	Medium	Min.	Typ.	Max.	Unit
Operating voltage	*Electrical*	*4.5*	*5.0*	*5.5*	*V*
Wavelength	*Optical*	*640*	*650*	*670*	*nm*
Response delay to blocking of PWM signals	*Optical*		*70*	*78*	*ns*
	Electrical		*40*	*50*	*ns*
	RealSync		*0.25*		*µs*

Table 22. Performance specifications of the inter-locking.

Fault input / output flags are also available on the digital connectors (A/B/C/D) located at the rear side of the B-Box. These signals are logically grouped into one fault when entering the fault manager (see Fig. 13). The output directly replicates the nFLT_OUT inter-lock signal.

Pin	Signal	Level	Pin	Signal	Level
A33	*nFLT_A_IN*	*3.3 V*	*A67*	*nFLT_OUT*	*3.3 V*
B33	*nFLT_B_IN*	*3.3 V*	*B67*	*nFLT_OUT*	*3.3 V*
C33	*nFLT_C_IN*	*3.3 V*	*C67*	*nFLT_OUT*	*3.3 V*
D33	*nFLT_D_IN*	*3.3 V*	*D67*	*nFLT_OUT*	*3.3 V*

Table 23. Signal assignment for the nFLT I/O flags on A/B/C/D slots.

FAULT MANAGER

At the firmware level, all fault signals are grouped inside the fault manager, which manages the overall system execution state and controls the activation of the PWM outputs
The collected fault signals include:

- Dedicated fault input lines FLT 0..15 (digital connector A)
- Fault signals on digital I/O connectors (A, B, C and D) (active low signals, inhibited by default)
- Interlocks (optical and electrical)
- Overvalues on analog inputs AIN 0..15
- Watchdog counter

BBOS allows to configure the enabling/disabling of each digital fault input line individually through a configuration mask. Reciprocally, interlocks and analog input protections must be configured using the B-Box front panel and the LCD screen. All signal values (fault flags) can be read from the corresponding VALUES register.

The wachdog counter (WDG) is automatically configured with a period of 2.5 times the control processing period. A fault is raised when no data is received by FPGA logic within this interval.

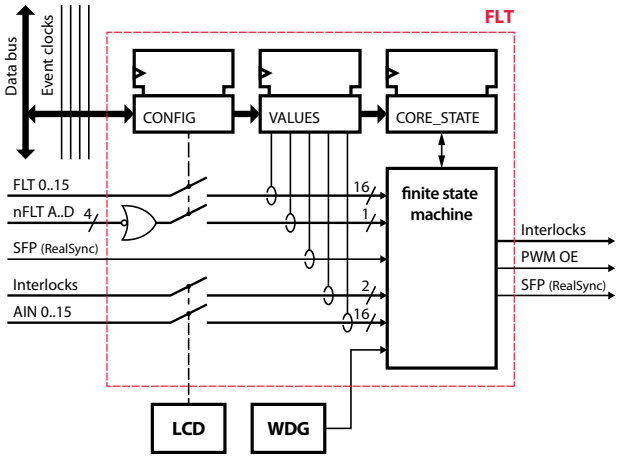


Fig. 13. Internal structure of the FLT peripheral block.

1 Optionally and when relevant, electrical or optical inter-locks can be wired as well, such as to reduce the response time to faults.

CLOCK AND INTERRUPT GENERATORS

Four independent clock generators are available on B-Box. They allow to configure independent time bases that can be allocated to various FPGA peripherals. This guarantees a very strict management of frequencies and phase-shifts between blocks. Clock generators support glitch-less re-configuration during run-time (variable-frequency).

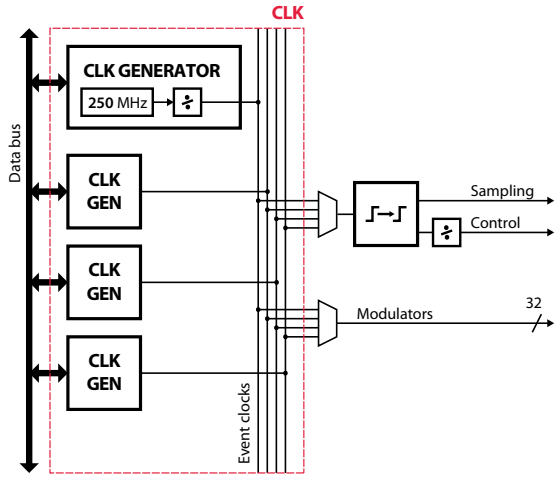


Fig. 14. Internal structure of the CLK peripheral block.

Outputs of clock generators are either interrupt signals or reference clocks for pulse-width modulators. Typical configurations include:

» **Basic example**: Control, modulation and sampling are at the same frequency. All resources are mapped onto the same clock generator. Measurements are made in the middle of the current ripple.

» **Multi-frequency example**: Two distinct converters are switching at different frequencies (e.g. 4 kHz and 5 kHz). Sampling is done at a common multiple (e.g. 20 kHz).

» **Variable-frequency**: One variable-frequency generator is used for modulation. Another frequency generator is used at a constant frequency for sampling and control.

Characteristic	Value
Counter resolution	*4.0 ns*
Counter depth (carrier, prescaler)	*16 bits*
Postscaler value (IRQ subsystem)	*0 – 4095*
Achievable frequency range	*58.2 mHz – 250 MHz*

Table 24. Performance specifications of the CLK peripheral block.

In a multi-device configuration (with stacked B-Boxes), all clock generators are intrinsically syntonized and automatically synchronized. This way, all phase-dependent operations such as sampling (ADC) or modulation (PWM) are guaranteed to have extremely accurate timings. Achievable performance is shown in Table 25 and illustrated in Fig. 15.

Characteristic	Min.	Typ.	Max.	Unit
Mean deviation, any slave B-Box vs. master	*-2.0*	*0*	*2.0*	*ns*
Phase noise (jitter), any B-Box, 3σ		*± 230*		*ps*

Table 25. Synchronization performance of CLK peripheral blocks across multiple B-Boxes using *RealSync*.

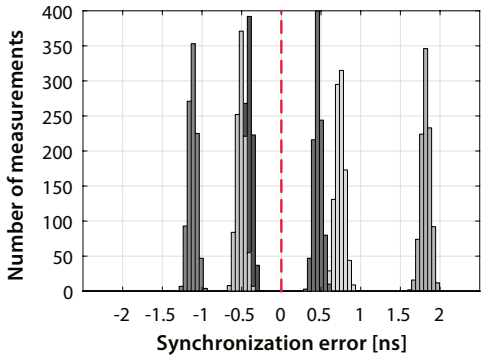


Fig. 15. Relative phase error performance with several B-Boxes in a stacked configuration (example with 6 slaves units).

PULSE WIDTH MODULATORS

The B-Box RCP embeds a full PWM signal generation system, featuring five sub-systems. Each of them generates 32 PWM signals. Fig. 16 depicts the corresponding structure:

- CB-PWM: Carrier-based modulators (32 channels). Various types of carriers are available, with single or double update rate. The CB-PWM block also provide hardware support for space-vector modulation (SV-PWM).
- PP-PWM: Programmed patterns modulators (2x three-phase). They allow the implementation of Selective Harmonic Elimination (SHE) or other types of Optimized Pulse Patterns (OPP).
- DO-PWM: Direct outputs. The direct access to the output state ('1' or '0') typically enables the implementation of software-modulated techniques such as Model Predictive Control (MPC). This also allows to use PWM outputs as standard digital outputs (possibly with dead time).
- SS-PWM: Sort-and-Select modulation and balancing (2 arms of up to 8 modules). This sub-system offers hardware-level support for the operation of Modular Multilevel Converters or similar topologies.
- SB-PWM: This subsystems connects with the user-programmable area (sandbox), which allows for the implementation of fully-customized modulation techniques. Easy-to-use I/O access from the software level is offered by the SBI and SBO blocks (see page 16).

At the output, each of the 32 PWM signals can be directly propagated to the physical outputs (electrical or optical), or to go through a dead time generator.
This results in 32 PWM lanes. By default, lanes are also arranged into 16 pairs of adjacent lanes designated as channels. Within a channel, odd lanes are always low-side signals, while even lanes are always high-side. PWM lanes #0-31 are available from the electrical connectors, while only PWM lanes #0-15 are produced on the optical outputs.
Dead time is obtained by delaying the rising edge of each PWM signal within a given pair. This results in an equivalent propagation delay of half the dead time.

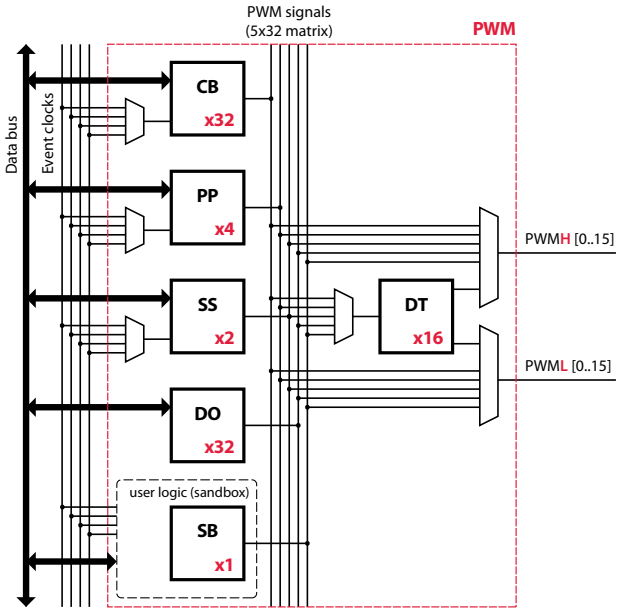


Fig. 16. Internal structure of the PWM signals generation block.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 26. Performance specifications of the dead time generation.

Channel	0	1	2	...	7	8	9	10	...	15
Lane	*0*	*2*	*4*	*...*	*14*	*16*	*18*	*20*	*...*	*30*
	1	*3*	*5*	*...*	*15*	*17*	*19*	*21*	*...*	*31*

Table 27. Designation of the PWM lanes and channels.

CB-PWM: CARRIER-BASED MODULATION

Carrier-based modulators offer the simplest way to generate pulse-width modulated signals. The corresponding subsystem features 32 independent modulators, which offer independent duty-cycle and phase parameters as well as four different types of carriers. With triangular carriers, modulators can be configured with single or double update rates (once or twice per PWM period).

Characteristic	Value
Counter depth	*16 bits*
Edge resolution (counter resolution)	*4 ns*

Table 28. Performance specifications of the CB-PWM block.

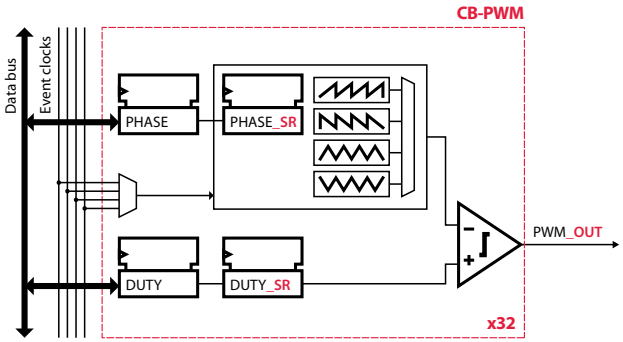


Fig. 17. Internal structure of the CB-PWM peripheral block.

SV-PWM: SPACE VECTOR MODULATION

Space vector modulation (sometimes referred to as SVM) is supported through dedicated software drivers, making use of the same resources as the CB-PWM subsystem. Indeed, once the closed vectors have been identified and the suitable sequence determined, the switching events can be easily produced by suitably-programmed modulators. SV-PWM automatically configures adjacent lanes or channels and supports single or double update rates.

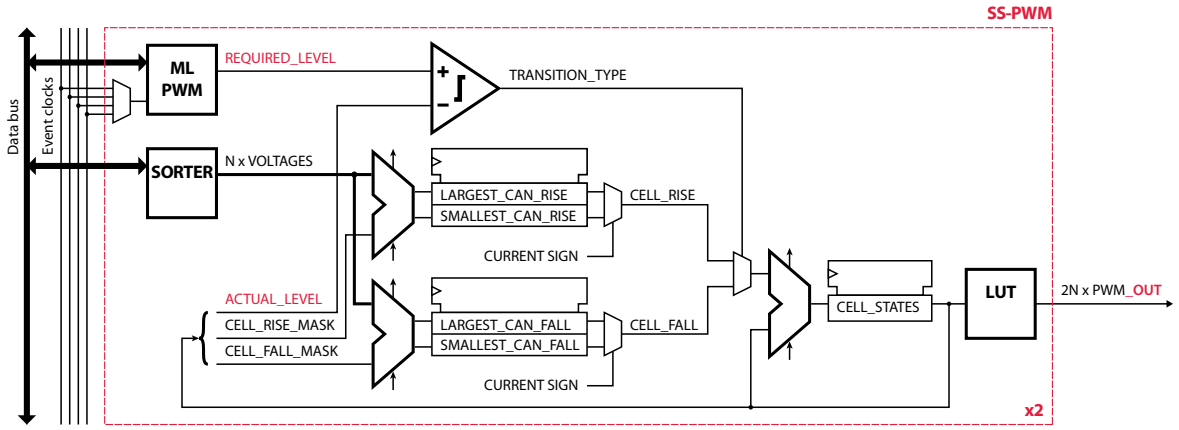


Fig. 25. Internal structure of the SS-PWM peripheral block.

SS-PWM: SORT-AND-SELECT MODULATION FOR MODULAR MULTILEVEL CONVERTERS (MMC)

Modulation with integrated voltage balancing for multilevel converters is supported at the firmware level thanks to the SS-PWM block. It applies to Modular Multilevel Converters as well as similar topologies with floating submodules.

This subsystem accesses the voltages acquired on the analog inputs in order to sort the submodule voltages and allocate the switching events to the suitable submodule as a function of the current polarity.

The SS-PWM block is compatible with half- and full-bridge submodule topologies and hence with both positive and negative arm voltages. The pre-implemented solution also guarantees that only one submodule switches at a given time in order to minimize switching losses and optimize the ratio between apparent and actual switching frequencies. Finally, the firmware also supports the exclusion of one or several submodules from the modulation process, as required by most fault-tolerant operation mechanisms.

Characteristic	Symbol	Value
Number or submodule per converter arm	*N*	*4, 8, 16 (–bypass)*
Number of output voltage levels	*L*	*N+1 or 2N+1*
Switching frequency range	f_{sw}	*3.72 Hz – 1 MHz*
PWM edge resolution		*20 ns*

Table 29. Performance specifications of the SS-PWM block.

SB-PWM: PWM ACCESS FROM THE SANDBOX

In addition to existing modulators, the B-Box also features a user-programmable area inside the FPGA . This notably allows to implement special own modulation techniques. In this sandbox, data read and write access from / to the CPU is provides from the the SBI and SBO blocks, respectively (see "User-programmable area (Sandbox)" on page 16).

The SB-PWM subsystem itself allows to connect to the PWM lanes through the dead-time generator block (see Fig. 16) as well as the B-Box's hardware protection mechanisms.

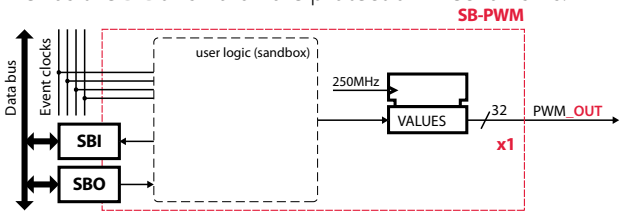


Fig. 18. Internal structure of the SB-PWM block.

DO-PWM: DIRECT OUTPUT ACCESS

Direct access to the PWM outputs is supported by the DO-PWM subsystem. It distinguishes from the SB-PWM in the sense that it is pre-implemented and requires no HDL editing. PWM state values (0 or 1) can be written directly from the CPU cores. This may typically be useful for model-predictive control (MPC) or sliding mode control techniques such as direct torque control (DTC).

Similarly to all PWM subsystems, when used as a channel, output lanes benefit from the dead-time generator block as well as protective mechanisms.

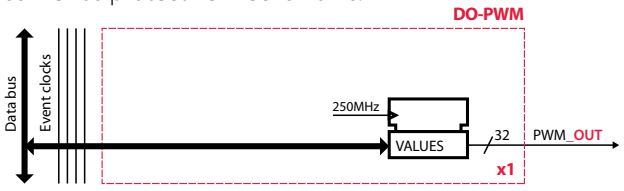


Fig. 19. Internal structure of the DO-PWM block.

PP-PWM : PROGRAMMED PATTERNS MODULATION

The programmed pattern blocks support modulation techniques that rely on pre-defined switching instants such as the generation of firing angles on a thyristor-based converter, the implementation of Selective Harmonic Elimination (SHE) or any Optimized Pulse Pattern (OPP). Three-phase system are supported.

PP-PWM have a fixed counter period (hence angular resolution), but can nevertheless be fed by variable-frequency clocks (see CLK peripheral block), typically aiming to be integrated withing a software PLL.

Each PP-PWM block contains several look up tables (LUT) for switching angles, registers for indicating the direction (up or down) of each switching event, as well as an additional truth table for decoding the output state.

The PP-PWM blocks are meant for accelerating the run time execution of OPP-based modulation and not for supporting the computation of the associated optimization algorithms.

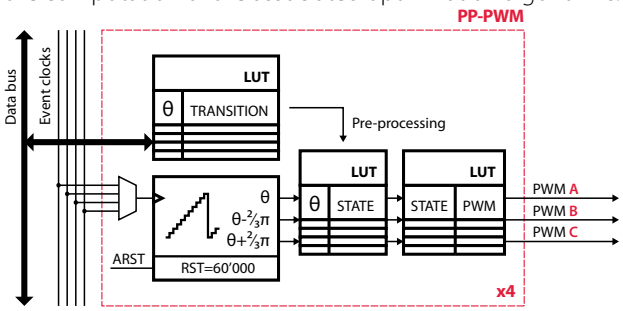


Fig. 20. Internal structure of the SS-PWM block.

Characteristic	Value
Number of angle registers (values 0 – 60'000)	*3x 16 angles x 16 bits*
Number of transition direction bits registers (up or down)	*3x 16 bits*
Size of output LUT	*t.b.d.*
Edge resolution (respectively to signal period)	*0.017 ‰*

Table 30. Performance specifications of the PP-PWM block.

DEAD TIME GENERATION SUBSYSTEM

As depicted by Fig. 16, the PWM block features a dead time generator at its output. This subsystem can be either used or bypassed by picking-up the signals from the PWM signals matrix directly (outputs of the modulators). Signals from all five PWM subsystems can be routed to the physical outputs (electrical or optical).

The dead time generation relies on a finite state machine operating as depicted in Fig. 21. Essentially, rising edges of the high-side and low-side signals are delayed by a programmable amount of time. This results in an equivalent propagation delay of half the dead time.

Intrinsically, this implementation guarantees that a pulse shorter than the dead time value is not produced.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 31. Performance specifications of the dead time generation.

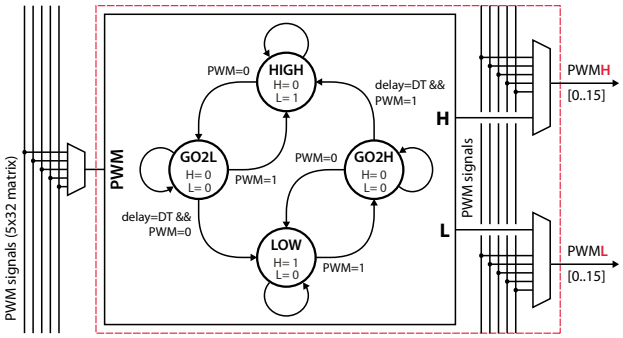


Fig. 21. Internal structure of the dead time generation block.

DATA TRANSFER PERFORMANCE

The transfer of continuously-updated modulation parameters from the processing core to the distributed modulators causes delays, which depend on the amount of data to be transferred. Fig. 22 shows the achieved performance with respect to the update of the CB-PWM block. Other modulators perform similarly.

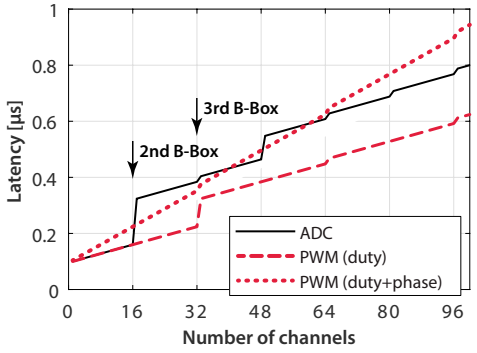


Fig. 22. Data transfer delay, as a function of the number of channels and number of B-Boxes.

INCREMENTAL POSITION DECODERS

The B-Box RCP features decoder inputs for quadrature-encoder speed / position sensor signals (usually called A and B), with or without a reset line (usually called Z). These inputs are either configurable as four independent inputs or two differential inputs.

Each decoder module counts all 4 edges of the A and B inputs, leading to an angular resolution 4 times superior to the PPR value usually specified for a given encoder. The position counter can be reset either at a specified value, or using the Z signal provided by the sensor.

Finally, the position can be latched similarly and simultaneously to the sample and hold feature of the ADC inputs, or simply read at the start of the data transfers to the CPU.

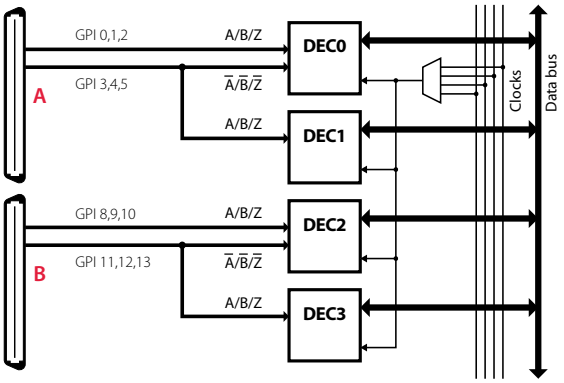


Fig. 23. Device mapping and configuration of the four incremental speed / position sensors decoders.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input signals	• *Single-ended signalling : A, B and Z (Z is optional)* • *Differential signalling : A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$ ($\overline{Z}$ are optional)*				
Sampling options	*Either synchronized with ADC, or independent*				
PPR frequency	*Quadruple rate.*	*0*		*5*	*MHz*

Table 32. Performance specifications of the DEC block.

CAN TRANSCEIVER

An isolated TJA1041 Controller Area Network (CAN) transceiver is available for communication between B-Box and third-party devices. Connectivity is provided through an RJ45 connector on the rear side of the device.

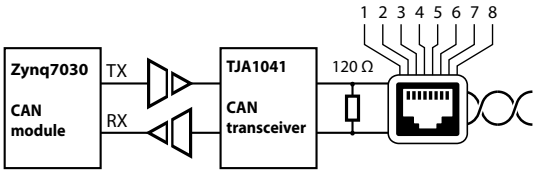


Fig. 24. Block diagram of the Controller Area Network peripheral.

Characteristic	Min.	Typ.	Max.	Unit
Operating baudrate			*1.0*	*MBd*
Tolerable voltage on CAN+ and CAN- pins	*-27*		*+40*	*V*
Bus impedance	*119*	*120*	*123*	*Ω*

Table 33. Performance specifications for the CAN transceiver.

Pin	Color	Description	Pin	Color	Description
1	*orange stripe*	*CAN H*	*5*	*blue stripe*	*NC*
2	*orange solid*	*CAN L*	*6*	*green solid*	*GND*
3	*green stripe*	*GND*	*7*	*brown stripe*	*NC*
4	*blue solid*	*NC*	*8*	*brown solid*	*NC*

Table 34. CAN pin/pair assignments.

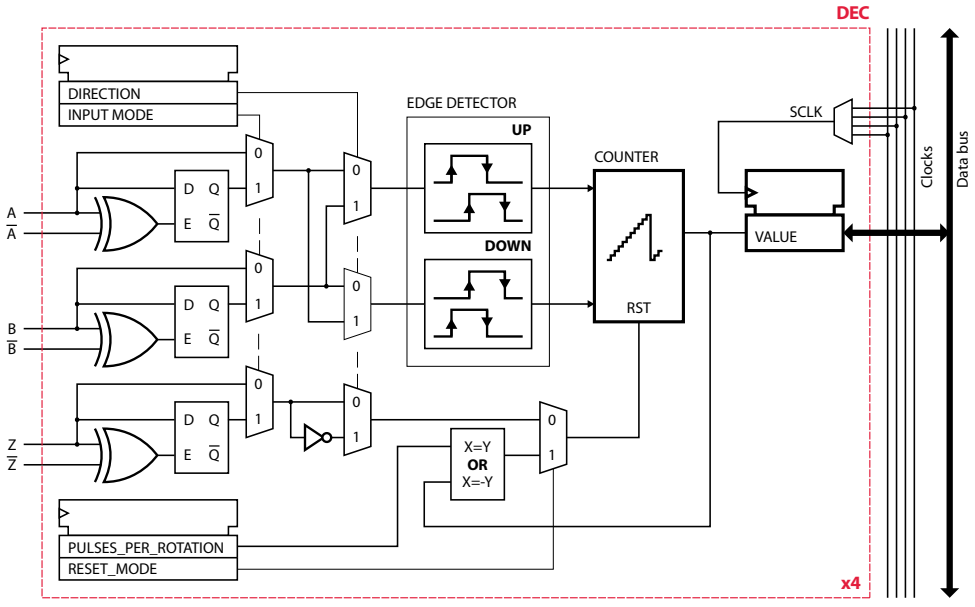


Fig. 26. Internal structure of the DEC block.

USER-PROGRAMMABLE AREA (SANDBOX)

The B-Box RCP is designed such that its programmable logic area (PL) can embed user-defined logic. This may allow for the implementation of special modulation techniques, proprietary communication mechanisms, or interfacing with external hardware and components.

Within this special area, designated as *sandbox*, two peripheral blocks are pre-implemented for easy-to-use I/O access from / to the CPU cores :

» SBI : Input from the sandbox
» SBO : Output to the sandbox

Also, the sandbox offers connectivity to the following I/O :

» ADC values (16x 16 bits signed integers)
» SB-PWM signals (32 bits register)
» Internal clocks
» Physical I/Os (FLT, USR, GPI, GPO)

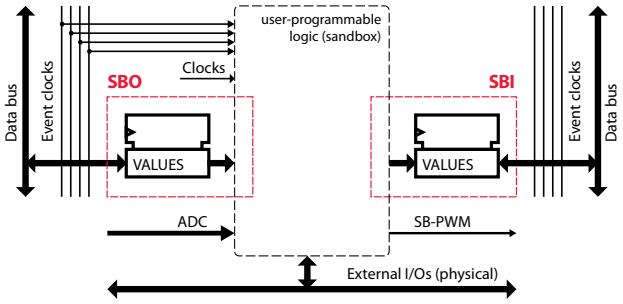


Fig. 27. Internal structure of the SBI and SBO blocks.

Thanks to the *RealSync* communication and synchronization protocol, the sandbox can be used indistinctively on the master or a slave B-Box within a control network. The data transfers (read or write) from the CPU core is handled by the SBI or SBO blocks using either the write-through (configuration) or write-back (real-time) data traffic, as with any other peripheral block.

C/C++ drivers (as well as their blockset counterparts) are readily available within the software development kits (SDKs). On the programmable logic side, development templates are provided upon request. In the provided HDL source code, other peripheral blocks are obfuscated.

ENVIRONMENTAL CONDITIONS

The B-Box RCP is designed to be supplied with a 60W 90–240VAC power supply. Other environmental conditions are specified in Table 35.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage		*90*		*240*	*V*
Power consumption		*5*		*60*	*W*
Inrush current				*0.7*	*A*
EMC performance	*IEC61000-3-2 class A*	*pass*			
Burst immunity	*IEC61000-4-4 Level 4*	*pass*			
Conducted immunity	*IEC61201-3 class A*	*pass*			
Operating temperature		*0*		*45*	*°C*
Storage temperature		*-10*		*85*	*°C*
Relative humidity	*Non-condensing*	*5*		*85*	*%*
Absolute humidity		*1*		*25*	*g/m³*

Table 35. Environmental specifications for the B-Box RCP.

MECHANICAL DATA

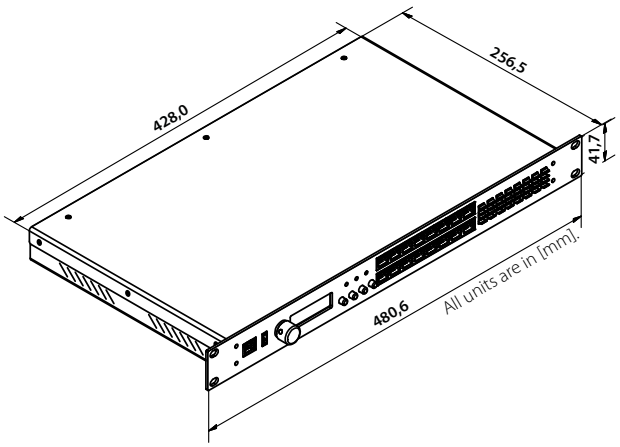


Fig. 28. Mechanical dimensions of B-Box RCP.

REVISION HISTORY

- » 18.05.19 : Preliminary version
- » 18.12.19 : DEC mapping updated, timing specifications added. Various fixes.
- » 11.02.20 : Additional details regarding the SBI, SBO and SB-PWM blocks.
- » 01.06.23 : Added information on GPO blocks. Modified company address.

This product must be used in electric / electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.
Caution, risk of electrical shock! When using the devices, certain parts of the modules may carry hazardous voltages (e.g. power supplies, busbars, etc.). Disregarding this warning may lead to injury and / or cause serious damage. All conducting parts must be inaccessible after installation.

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ABOUT US

Imperix Ltd is a company established in Sion, Switzerland. Its name is derived form the Latin verb imperare, which stands for controlling and refers to the company's core business: the control of power electronic systems. Imperix commercializes hardware and software solutions related to the fast and secure implementation of pilot systems and plants in the field of power conversion, energy storage and smart grids.

NOTE

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Data may change, as well as legislation, and the reader is strongly advised to obtain copies of the most recently issued regulations, standards, and guidelines.