INTERFACING OPAL-RT DOUT TTL/CMOS BOARD

DECIDING WHETHER OR NOT TO USE TERMINATION

(WHITE PAPER)

VERSION 1.2

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1. INTRODUCTION

Digital signals are the most common mode of communications used between computers and peripherals, instruments, and other electronic equipment because they are, of course, fundamental to the computer's operation. Over the years, the devices used to carry out logic functions have changed considerably. An early family of devices were simple switches, which gave way to relays. These, in turn, were superceded by diodes and eventually transistors. **T**ransistor to **T**ransistor **L**ogic (**TTL**) [1] remained popular for a relatively long period of time and even today is favored for certain applications. The invention of Field Effect Transistors (FETs), and in particular **C**omplementary **M**etal **O**xide **S**emiconductor Transistors (**CMOS**) [2] FETs changed basic logic design.

1.1 AIM OF THE DOCUMENT

This paper deals with two of the most commonly used signaling, the TTL and CMOS, and intends to briefly present their properties, and some recommendations when considering interconnecting OPAL-RT 32 Digital Inputs/Outputs TTL/**CMOS** boards[3] with third-party devices or User ECUs in order to ensure a good signal integrity over transmission lines with a matching scheme to absorb any reflections that may be generated by the source, the driver or the load, the receiver.

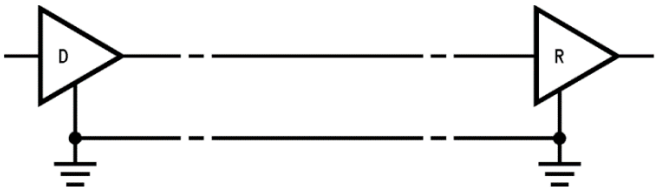


Figure 1: Unbalanced (single ended) Data Transmission

- **D**river OP5352 (126-0429), 32TTL out: 5V or 3V3,
- **R**eceiver OP5351 (126-0430), 32TTL in: 5V or 3V3.

[1] These chips have gates constructed of bipolar transistors using low internal voltages.

[2] Uses metal oxide semiconductor field effect transistors (MOSFETs) instead of bipolar transistors

[3] The I/O boards are based on the CMOS device : SN74LVC1G125DBVR (Low voltage CMOS logic)

Unbalanced data transmission uses a single conductor, with a voltage referenced to signal ground (common) to denote logical states. In unbalanced communication only one line is switched. **The advantage of unbalanced data transmission** is when multiple channels are required, a common ground can be used. This minimizes cable and connector size, which helps to minimize system cost. **The disadvantage of unbalanced data transmission** is in its inability to reliably send data in noisy environments. This is due to very limited noise margins. The sources of system noise can include externally induced noise, cross talk, and ground potential differences.

However, the paper also, but more succinctly, introduces the RS-422 and the LVDS standard to transmit digital signals over longer distances than could possibly do either CMOS or TTL. Finally, the paper presents OPAL-RT DIO push-pull solutions for system-to-system applications involved with higher voltages.

1.2 LOGIC LEVELS:

1.2.1. STANDARD LOGIC LEVELS AND LOGIC FAMILIES

The most commonly used bipolar logic family is transistor-transistor logic (TTL). But, there are many different TTL families, with a range of speed, power consumption, and other characteristics.

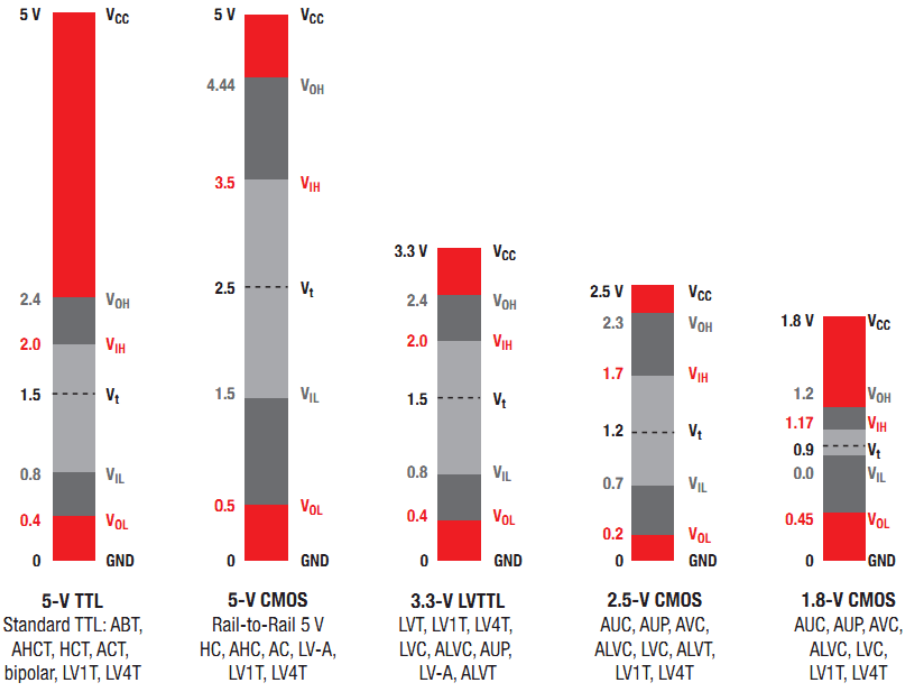


Figure 2: Standard Logic Levels[4]

The standard specifies the voltages for logic high and low for both the driver and receiver. A noise margin is built into the specification. The specifications for the signaling standards are essential in communication because they establish the voltage levels so that the driver and receiver agree with the logic high and low conditions.

[4] http://www.ti.com/lit/sg/sdyu001aa/sdyu001aa.pdf

1.2.2. TTL & CMOS I/O LEVELS

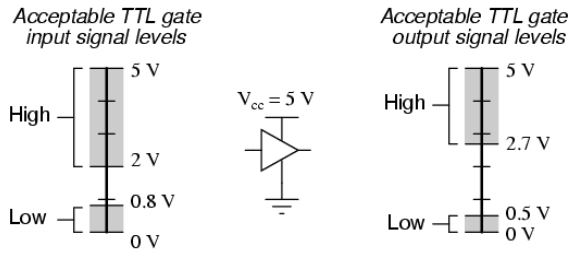


Figure 3: Acceptable TTL gate I/O levels

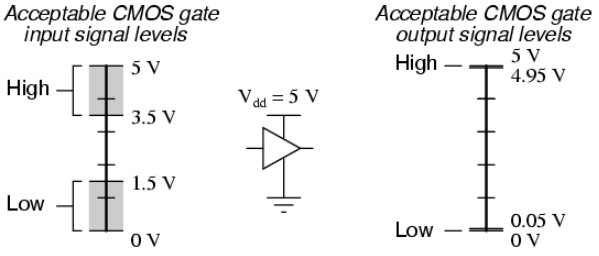


Figure 4: Acceptable CMOS gate I/O levels

If a voltage signal ranging between 0.8 volts and 2 volts were to be sent into the input of a TTL gate, there would be no certain response from the gate. Such a signal would be considered *uncertain*, and no logic gate manufacturer would guarantee how their gate circuit would interpret such a signal.

As you can see, the tolerable ranges for output signal levels are narrower than for input signal levels, to ensure that any TTL gate outputting a digital signal into the input of another TTL gate will transmit voltages acceptable to the receiving gate. The difference between the tolerable output and input ranges is called the *noise margin* of the gate. For TTL gates, the low-level noise margin is the difference between 0.8 volts and 0.5 volts (0.3 volts), while the high-level noise margin is the difference between 2.7 volts and 2 volts (0.7 volts). Simply put, the noise margin is the peak amount of spurious or "noise" voltage that may be superimposed on a weak gate output voltage signal before the receiving gate might interpret it wrongly.

It should be obvious from these figures that CMOS gate circuits have far greater noise margins than TTL: 1.45 volts for CMOS low-level and high-level margins, versus a maximum of 0.7 volts for TTL. In other words, CMOS circuits can tolerate over twice the amount of superimposed "noise" voltage on their input lines before signal interpretation errors result. CMOS noise margins widen even further with higher operating voltages[5]

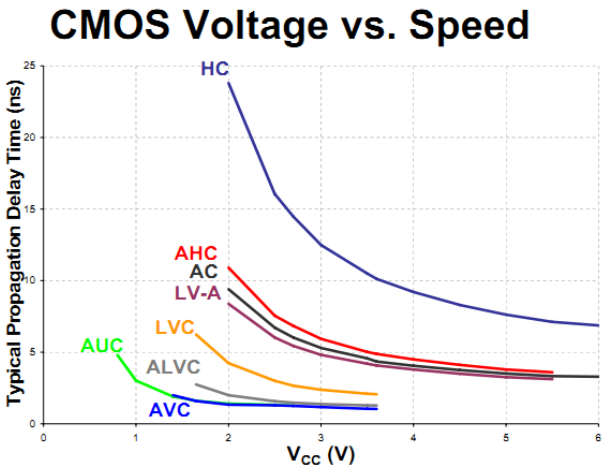


Figure 5: CMOS Voltage vs. Speed[6]

[5] http://www.web-books.com/eLibrary/Engineering/Circuits/Digital/DIGI_3P10.htm

[6] http://www.siongboon.com/projects/datasheet/logic%20gates%20&%20family%20selection%20guide%20(ti).pdf

1.2.3. INTERFACING TTL / CMOS AND VICE VERSA:

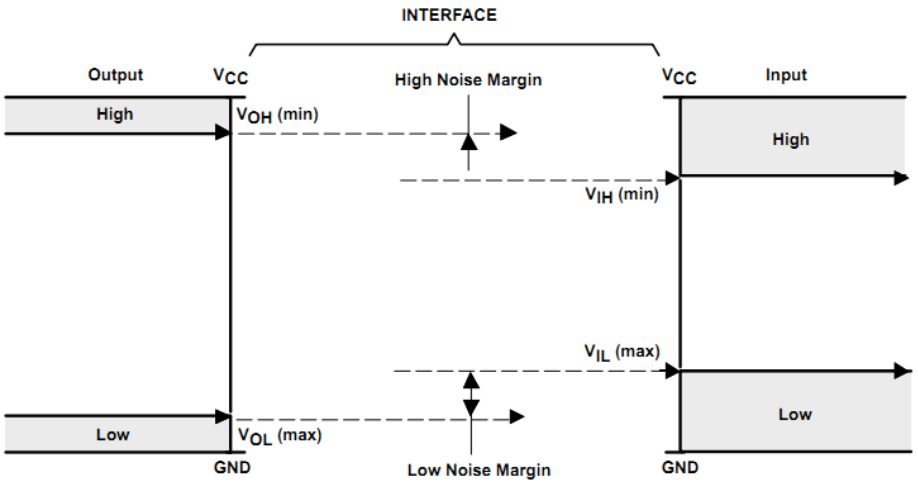
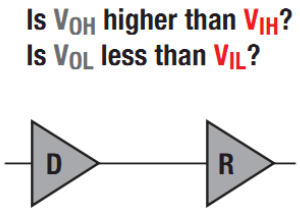


Figure 6: Logic Compatibility between I/Os

- VIHmin -- the minimum input voltage which will be accepted as a logic 1 state.
- VILmax -- the maximum input voltage which will be accepted as a logic 0 state.
- VOHmin -- the minimum output voltage representing a logic 1 state.
- VOLmax -- the maximum output voltage representing a logic 0 state.



D \ R	5 TTL	5 CMOS	3 LVTTL	2.5 CMOS	1.8 CMOS
5 TTL	Yes	No	Yes*	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes*

* Requires V_{IH} Tolerance

Figure 7: Comparison of Switching Standards

1.2.3.1. TTL DRIVING CMOS

Driver / user /TTL & Receiver / OPAL-RT /CMOS

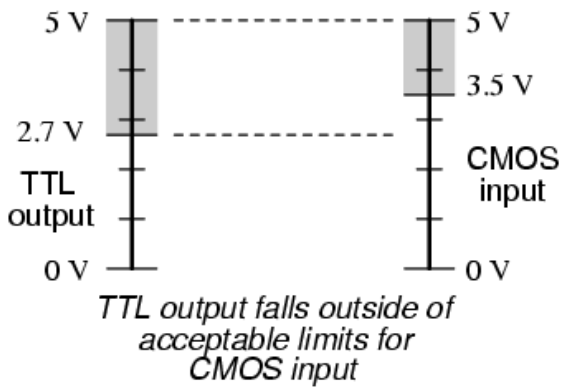


Figure 8: TTL driving CMOS without a Rpull-up

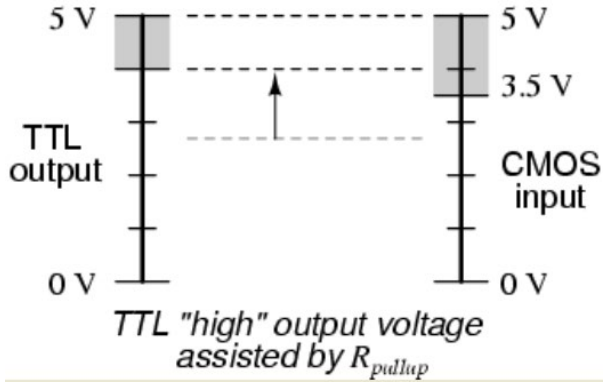


Figure 9: TTL driving CMOS with a Rpull-up

Given this mismatch (See Figure 7), it is entirely possible for the TTL gate to output a valid “high” signal (valid, that is, according to the standards for TTL) that lies within the “uncertain” range for the CMOS input, and may be (falsely) interpreted as a “low” by the receiving gate. An easy “fix” for this problem is to increase the TTL gate’s “high” signal voltage level by means of a pull-up resistor[7]:

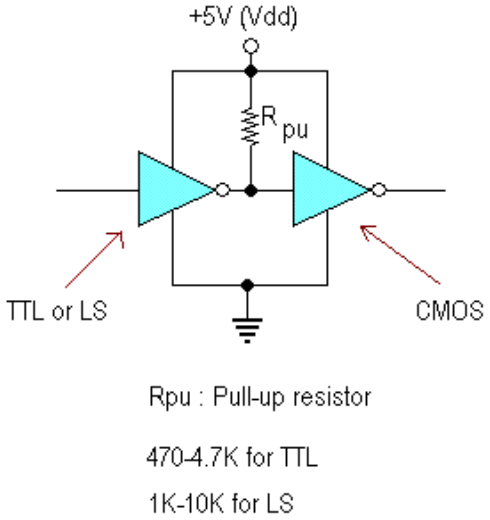


Figure 10: TTL to CMOS interface, assisted by a pull-up

[7] Already installed on OPAL-RY DOUT TTL/CMOS; 4K7 Ω.

1.2.3.2. CMOS DRIVING TTL

According to fig.8, there is compatibility, so the interface does not need any assistance.

Driver / OPAL-RT /CMOS & Receiver / user /TTL

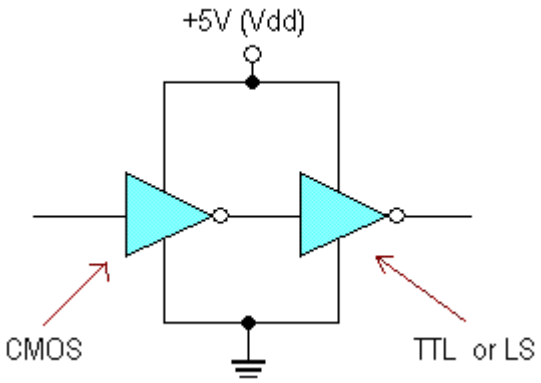


Figure 11: CMOS to TTL interface

1.2.4. TTL vs. CMOS

The main advantage of CMOS over TTL was the very low power consumption and small size. However, the speed at which they could switch was considerably slower and produced longer propagation delays. With time, TTL devices that consumed much less power, and CMOS devices that could switch faster have blurred the line between the two types, leaving size as the major difference.

Detail comparison[8]

Characteristics of CMOS logic:	**CMOS compared to TTL:**
• Dissipates low power: The power dissipation is dependent on the power supply voltage, frequency, output load, and input rise time. At 1 MHz and 50 pF load, the power dissipation is typically 10 nW per gate. • Short propagation delays: Depending on the power supply, the propagation delays are usually around 25 ns to 50 ns. • Rise and fall times are controlled: The rises and falls are usually ramps instead of step functions, and they are 20 - 40% longer than the propagation delays. • Noise immunity approaches 50% or 45% of the full-logic swing. • Levels of the logic signal will be essentially equal to the power supplied since the input impedance is so high. • Voltage levels range from 0 to VDD where VDD is the supply voltage. A low level is anywhere between 0 and 1/3 VDD while a high level is between 2/3 VDD and VDD.	1. CMOS components are typically more expensive than TTL equivalents. However, CMOS technology is usually less expensive on a system level due to CMOS chips being smaller and requiring less regulation. 2. CMOS circuits do not draw as much power as TTL circuits while at rest. However, CMOS power consumption increases faster with higher clock speeds than TTL does. Lower current draw requires less power supply distribution, therefore causing a simpler and cheaper design. 3. Due to longer rise and fall times, the transmission of digital signals becomes simpler and less expensive with CMOS chips. 4. CMOS components are more susceptible to damage from electrostatic discharge than TTL components.

[8] http://digital.ni.com/public.nsf/allkb/2D038D3AE1C35011862565A8005C5C63

2. CABLE CAPACITANCE VS. DRIVE CURRENT

In the past, digital design ignored the transmission line effects of logic interconnections. Generally, as long as the round trip propagation delay of a signal trace or cable was small as compared to the rise time of the digital signal, the reflections generated on the line were ignored and not terminated[9]. The length of the transmission path was assumed to be infinitely short. No reflections can occur on an infinitely short line since there is no propagation time between a signal and its reflection from the end of the line. A transmission line can be considered to be ***short*** if its electrical length $l_{electrical}$ is less than 1/6 of the rise time (T_{rise}) of the digital signal [see eq.1].

The line is short if:	$l_{electrical} < \frac{T_{rise}}{6}$, Equation **1**

So, when interfacing OPAL-RT boards with user ECUs, which are connected by a cable, do not take long cables for granted. You may not be getting all the high frequency signals through them you think you are. Also, your driving device may be running into trouble due to exceeding its current capabilities trying to drive the cable at high frequencies. It can reach its slew rate limit resulting in noticeable distortion.

That's why, when using TTL as a driver gate, especially totem pole outputs could be a challenge due to low current drive level: 400 µA in sourcing and 1.6 mA in sinking.

Considering a 5V TTL with IOH of 400 µA switching at 50 kHz and a cable capacitance of 30 pF/ft, how long can you drive a signal prior to facing signal integrity degradation?

Vmax (5V TTL)	5.0E+0	C (pF)	25.5E-12	
Freq (Hz)	100.0E+3	C cable pf/ft	30.0E-12	
Slew rate V/s	3.1E+6	Length (ft)	848.8E-3	
SR V/µs	0.3142	1 ft	0.3048	1 m
I TTL driver (A)	400.0E-6	Max cable length (m)	**258.7E-3**	

SR (Slew Rate) = 2*Pi*Freq*Vmax; C= i/ (SR*Vmax) [no Resistor is inserted].

[9] H. Johnson and M. Graham, High-Speed Digital Design. Upper Saddle River, NJ: Prentice Hall, pp.2, 166-167.

So, in order to transmit signals at 100 kHz users should use cables with a maximum length of 26 cm, above may cause distortion. Reducing the frequency to 10 kHz will increase the cable length to 2.6 m.

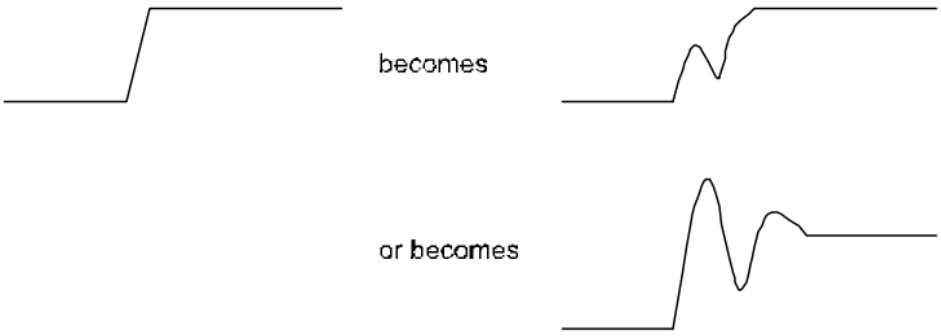


Figure 12: Typical waveform distortions

The maximum frequency that can be transmitted over a given length of cable is a function of both the cable[10] capacitance and the ratio of the maximum peak signal voltage to the current available from the constant current source:

Drive Current	Cable Length @30 pF/ft	Frequency Response ±5%	
		Output Signal Amplitude	
mA	Ft.	± 1V	± 5V
2	10	500 kHz	50 kHz
	100	80 kHz	16 kHz
	1000	8 kHz	1.7 kHz
5	10	600 kHz	200 kHz
	100	150 kHz	50 kHz
	1000	25 kHz	5 kHz
10	10	700 kHz	300 kHz
	100	300 kHz	100 kHz
	1000	40 kHz	10 kHz
20	10	1300 kHz	900 kHz
	100	500 kHz	150 kHz
	1000	70 kHz	20 kHz

Table I: *Cable Driving Parameters vs. Limited Drive Current*[11]

Even if the table is intended for analog signal stimuli, it gives a good idea of the maximum length cable (30 pF/ft) and also it shows that for a certain drive current, the slower the frequency, the longer the cable.

[10] RG58/U coaxial cable

[11] http://www.a-tech.ca/doc_technote/Intro_Current_Source_Power_Unit.pdf

The following formula gives a good assessment of the maximum frequency achievable for a fixed voltage, cable capacitance, and current drive available:

$$f = \frac{K}{2\pi C\left(\frac{V}{Icc - Ib}\right)}$$

Where:
f = Maximum frequency in Hz
$K = 3.45 \times 10^9$. K is the scale factor to convert Farads to picoFarads and Amperes to milliAmperes and a factor to allow cable capacitance to charge to 95% of the final charge.
C = Cable capacitance in picoFarads
V = Maximum peak measured voltage from sensor in volts
Icc = Constant current from current source in mA
Ib = Current required to bias the internal electronics, typically 1 mA

2.1. SOLUTIONS FOR INCREASING CABLE LENGTH

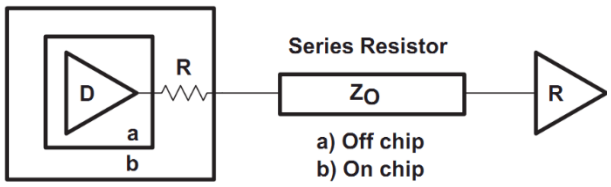
Here are several solutions for increasing the cable length. All of these solutions involve terms used in the calculations. Putting this another way: you must change the value of some term used in the calculations to use a longer cable. Of course you must recalculate the effect of each solution.

1. Use lower capacitance cable,
2. Use a driving device with a higher output capability (voltage and/or current),
3. Use a driving device with a lower output impedance (if its 50 Ohms that's the best you can do),
4. Reduce the load you are driving by dividing it up between outputs of a distribution amplifier,
5. Reduce the signal level over the cable run and put gain back in at the receiving end.

3. RECOMMENDED INTERCONNECT AND TERMINATION BOARD TO BOARD

Depending on the trace length, special consideration may need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system may appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections. We present here after five different techniques for terminating the outputs. The ideal situation is to identically match the impedance (ZO) of the cable and eliminate all reflections. In practice, however, exactly matching ZO is not always possible and settling for a close enough match that adequately minimizes the reflections may be the only option.

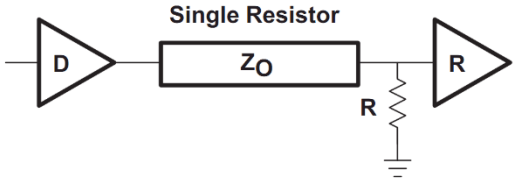
3.1 SERIES TERMINATION



It consists of a resistor in series with the output of the driving device and can be divided into two alternatives, depending on whether the resistor is physically located on or off the driving device. If the resistor is not located on the device, the value of the resistor should be R = ZO – ZD, where ZD is the output impedance of the driver, and the best placement is as close to the driver as possible. Although a delay occurs, no power increase is experienced and this technique has a relatively good noise margin.

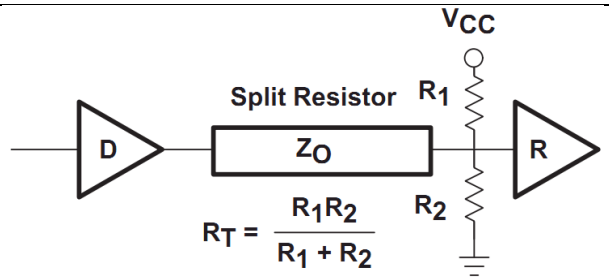
If the resistor is integrated on the device and part of the chip, its value is usually 25 Ω ≤ R ≤ 33 Ω. This setup has a slight delay, no increase in power, a good undershoot clamping, and is useful for point-to-point driving.

3.2 PARALLEL TERMINATION



It consists of a single resistor tied to GND. The ideal value of the resistor is R = ZO, and the best placement for it is as close to the receiver as possible. A heavy increase in power occurs, but no further delay is present. There is a relatively low dc noise margin in this configuration.

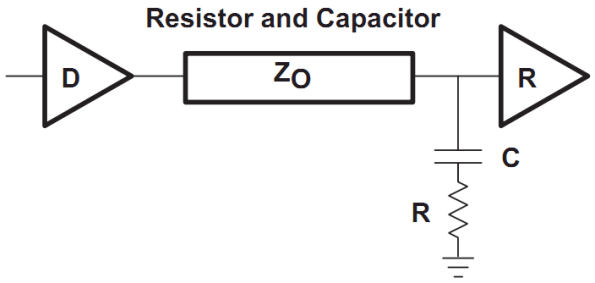
3.3 THEVENIN TERMINATION



It involves two split resistors; one resistor (R1) is tied to VCC and the other (R2) is tied to GND. The ideal value of the resistors is R1 = R2 = 2ZO; RT = (R1 x R2)/(R1 + R2), and the best placement for the resistors is as close to the receiver as possible.

It results in a heavy increase in power, with no delay being experienced, and is primarily used in backplane designs where proper drive currents must be maintained.

3.4 AC TERMINATION

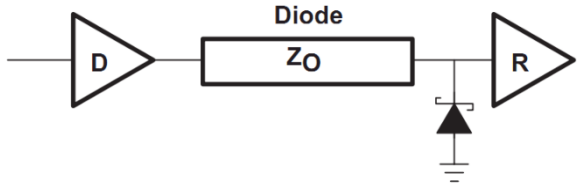


It has a capacitor in series with a resistor, both of which are running parallel to GND. The ideal value of the resistor

is R = ZO, and the value of the capacitor should be 60 pF < C < 330 pF. To determine the ideal value of the capacitor, it is recommended that a model simulation tool be used. The ideal placement of the resistor and capacitor is as close to the receiver as possible.

It has the highest amount of power consumed as the frequency increases, but no additional delay is experienced. Note that this termination technique can be optimized for only one given signal frequency.

3.5 DIODE TERMINATION



It consists of a diode to GND that should be located as close as possible to the receiver. An increase in power is not experienced, no delay occurs, and this configuration is useful for standard backplane terminations.

It is the most attractive of all techniques since there is no power increase and no delay occurs. However, since the delay associated with AC termination is so minimal and since no additional devices are required, whereas in all the other techniques at least one additional component is required, **it is usually the technique recommended by the Advanced System Logic department of Texas Instruments.**

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	SETS STATIC LINE LEVEL	DELAY	IDEAL VALUE	COMMENTS
Single resistor	1	Significant	Yes	No	$R = Z_O$	Low dc noise margin
Split resistor	2	Significant	Yes	No	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
Resistor and capacitor	2	Yes	No	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series resistor-off device	1	No	No	Yes	$R = Z_O - Z_D$	Good noise margin
Series resistor-on device	0	No	No	Small	$25 = < R = < 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

*Table **2**: Termination Techniques Summary*[12]

By properly choosing a termination matching the characteristic impedance (Zo) of the transmission line, the energy in a digital transmission line signal can be turned into heat before it reflects and interferes with other forward propagating signals.

4. SHOULD OPAL-RT BOARDS BE TERMINATED?

Although termination may be necessary in some situations, there are also disadvantages to implementing termination. Termination increases load on the drivers, increases installation complexity, changes biasing requirements and makes system modification more difficult.

> Note: If termination is added, and its effects on biasing are not considered, it can compromise the performance of the communications system.

The decision to whether or not to use termination should be based on the cable length and data rate used by the system. A good rule of thumb is if the electrical length[13] of a transmission line is less than the rising time of the signal / 6, termination is not needed. This rule makes the assumption that reflections will damp out in several trips up and down the data line.

[12] http://www.ti.com/lit/ml/scba010/scba010.pdf

[13] Electrical length is defined as the distance that a signal can travel in an electrical medium during the time that it takes for one rise or fall time, whichever is longer.

Transmission lines are defined by two parameters: characteristic impedance Z0 and delay time TD. What is the delay time? This tells you how long it takes a step voltage to travel from one end of the cable to the other. The **time delay** is easily determined by the **cable speed** and **cable length**.

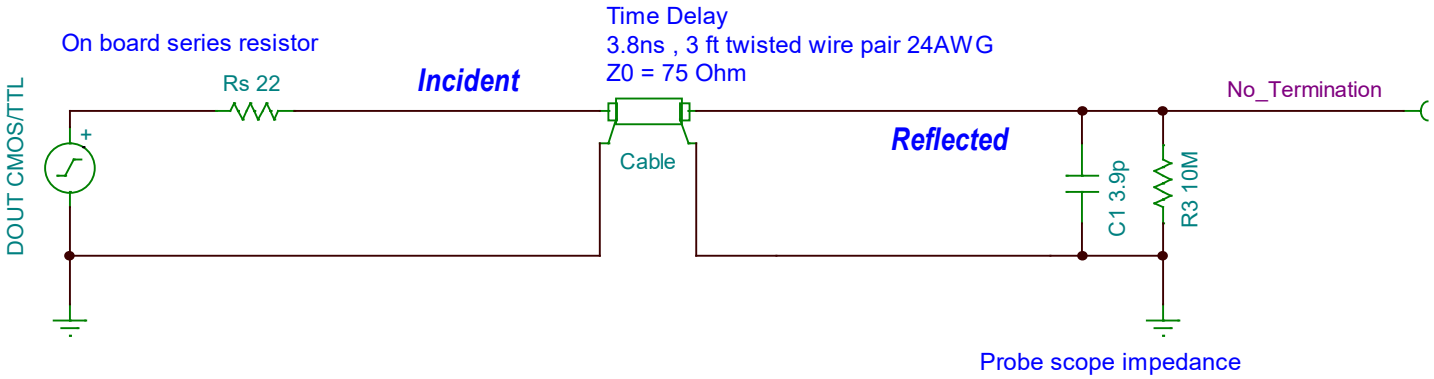


*Figure **13**:* DOUT CMOS / TTL has a, on board, 22 Ω series resistor.

The delay of a cable or velocity factor is determined by the dielectric constant of the cable. The following table gives common dielectric materials and their characteristics for coaxial cable:

Dielectric Material	Time Delay (ns/ft)	Propagation Velocity (% of c)	Propagation Velocity (formula needs single value) (% of c)	Time Delay ns/ft Worst case	Speed of light in free space
Solid Polyethylene (PE)	1.54	65.9	65.9	1.5417E-09	1.016E-09
Solid Teflon (ST)	1.46	69.4	69.4	1.4640E-09	
Foam Polyethylene (FE)	1.27	80	80	1.2700E-09	
Air Space Polyethylene (ASP)	1.15-1.21	84-88	84	1.2095E-09	

*Figure **14**: Common dielectric materials and their characteristics*[14]

To get the time delay of a twisted pair wire cable, one can use the following calculator[15]:

[14] http://www.gpssource.com/files/Cable-Delay-FAQ.pdf

[15] http://www.eeweb.com/toolbox/twisted-pair ; It also provides the calculus for a coax cable.

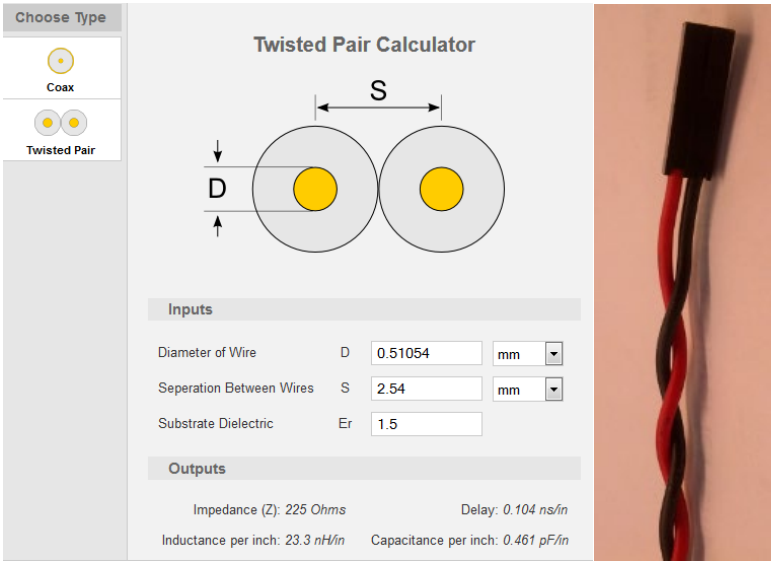


*Figure **15**: Example of a twisted pair wire 24 AWG terminated with 0.1' header (2.24 mm)*

The software gives a delay of roughly 0.104 ns/in. So considering 3 feet (0.9144 m) of a twisted pair wire, the time delay we get a delay of 3.78 ns.

The electrical length of a transmission line is given by:	$l_{electrical} = \frac{l_{physical}}{v_p}$, Equation 2
The speed at which signals propagate along a transmission line v_p is given by: ϵ_{eff} Dielectric material used in the transmission line, and c the speed of light.	$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}}$, Equation 3

For the example, the dielectric constant ϵ_{eff} is set to 1.5[16].

$$\Rightarrow \quad v_p = \frac{3\times10^8 m/s}{\sqrt{1.5}} = 245 \times 10^6 m/s$$

The electrical length

$$\Rightarrow \quad l_{electrical} = \frac{0.9144m}{245\times10^8 m/s} = 3.73\ ns$$

[16] "Another difficulty with the approximation involves the concept of "effective dielectric constant." The fields surrounding the wires exist partly in the dielectric insulation and partly in the air surrounding the whole configuration. The effective dielectric constant, therefore, lies between that of air, which is 1, and that of PTFE, which is 2. The exact value takes into account the relative proportions of field energy in those two substances. »

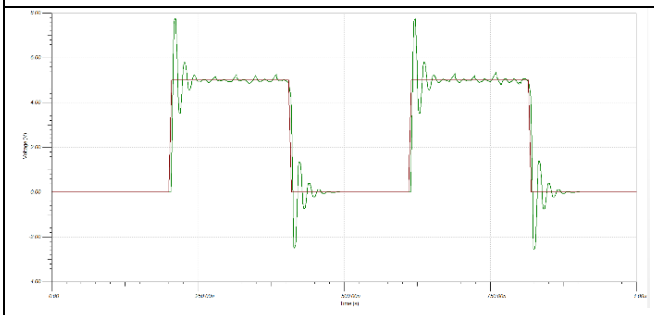
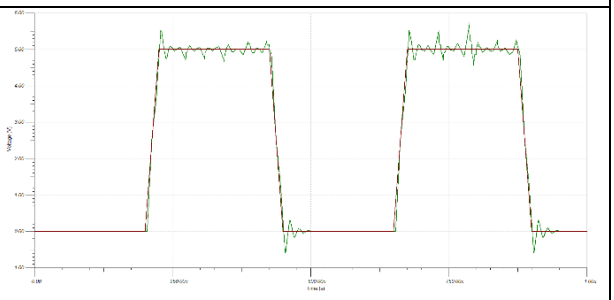
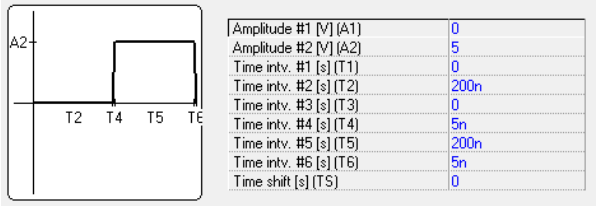
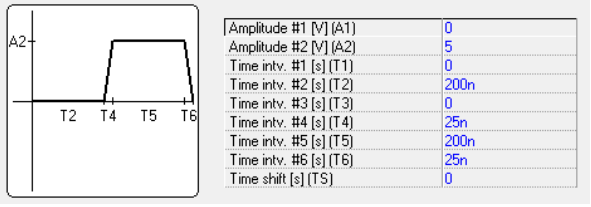
In the case of a digital signal, such OPAL-RT DOUT TTL/CMOS board, Trise≈1.5 ns [in stand-alone] and ≈20 ns when plugged on the OP5600, equation 1 yields:

$$\Rightarrow \quad 3.53ns \approx \frac{20ns}{6},$$

Since the electrical length of the line,$l_{electrical}$, is almost equal to 1/6 of the rise time of the signal, so considered *as a short line*, the line could possibly not be terminated. However, this is a theoretical approach, and it surely depends on the quality and the nature of the cables. Tuning is required and environment and equipment dependent.

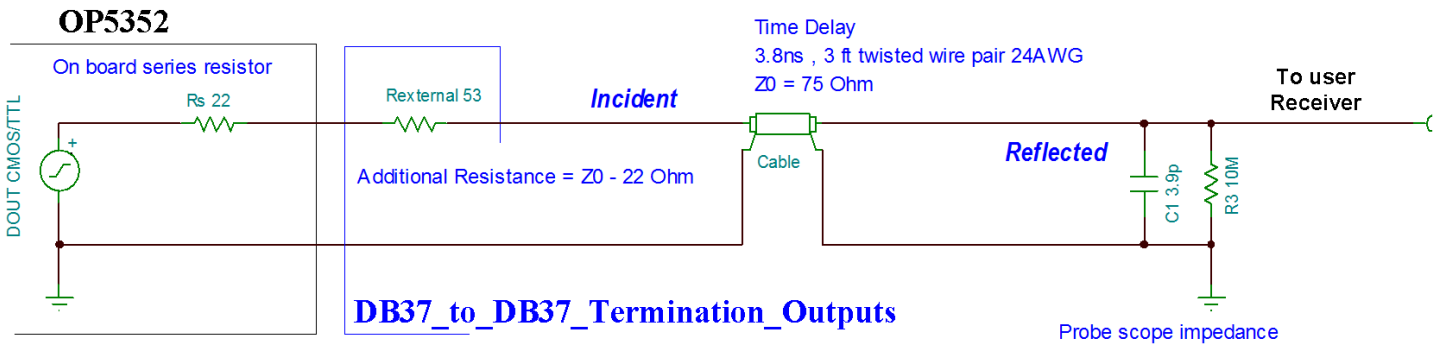
Simulation[17] can also be very helpful to assess whether or not to use a termination. For the comparison, the Time delay is set to 3.8 ns and two different rising times are set to observe the differences.

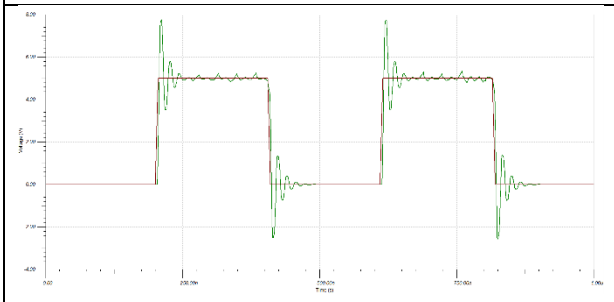
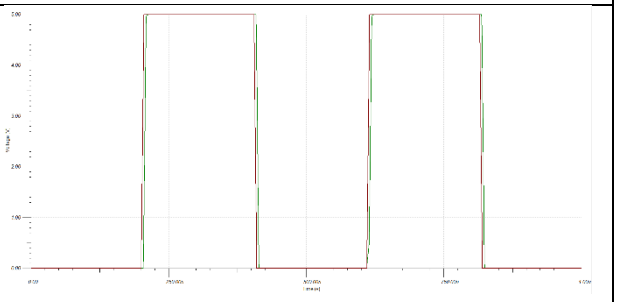
[17] TINA-TI Version 9.3.50.40 SF-TI

Not terminated & $l_{electrical} > \frac{T_{rise}}{6}$ T rise = 5 ns	Not terminated & $l_{electrical} < \frac{T_{rise}}{6}$ T rise = 25 ns
 Green waveform: Output: no termination	
The line model has a TD of 3.8 ns and a Zo=75Ω	
 A2 T2 T4 T5 T6 Amplitude #1 [V] (A1) 0 Amplitude #2 [V] (A2) 5 Time intv. #1 [s] (T1) 0 Time intv. #2 [s] (T2) 200n Time intv. #3 [s] (T3) 0 Time intv. #4 [s] (T4) 5n Time intv. #5 [s] (T5) 200n Time intv. #6 [s] (T6) 5n Time shift [s] (TS) 0	 A2 T2 T4 T5 T6 Amplitude #1 [V] (A1) 0 Amplitude #2 [V] (A2) 5 Time intv. #1 [s] (T1) 0 Time intv. #2 [s] (T2) 200n Time intv. #3 [s] (T3) 0 Time intv. #4 [s] (T4) 25n Time intv. #5 [s] (T5) 200n Time intv. #6 [s] (T6) 25n Time shift [s] (TS) 0

So, one can observe that no termination is theoretically required if the rule $l_{electrical} < \frac{T_{rise}}{6}$ is respected.

In case it is broken, we must terminate the link to ensure the integrity of the signal whatever the technique.



No termination: Time delay 3.8 ns and T rise = 5 ns	Termination: Rs technique Time delay 3.8 ns and T rise = 5 ns
	

Nota:

There is another rule of thumb still based on the cable length but also on the data rate. If the propagation delay of the data line is much less than one bit width, termination is not needed. This rule makes the assumption that reflections will damp out in several trips up and down the data line. Since the receiving UART will sample the data in the middle of the bit, it is important that the signal level be solid at that point. ***For example***, in a system with 2000 feet of data line the propagation delay can be calculated by multiplying the cable length by the propagation velocity of the cable. This value, typically 66 to 75% of the speed of light (c), is specified by the cable manufacture.

For our example, a round trip covers 4000 feet of cable. Using a propagation velocity of 0.66 × c, one round trip is completed in approximately 16 µs. If we assume the reflections will damp out in three *round trips* up and down the cable length, the signal will stabilize 18.5 µs after the leading edge of a bit. At 9600 baud one bit is 104 µs wide. Since the reflections are damped out much before the center of the bit, termination is not required.

5. ALTERNATIVES WHEN SYSTEM-TO-SYSTEM REQUIRES LONGER CABLE

Line drivers, such as those for RS-232, RS-422, RS-485, and LVDS, constitute a class of integrated circuits that interface two systems or devices over some distance, including point-to-point, multidrop, and bus and backplane applications. The need for such devices emerged in the early 1960s as the inherent limitations of sending high-speed signals over long distances using standard logic levels became apparent.[18]

OPAL-RT provides DIO solutions in a type B module [32DIO] for both RS-422 and LVDS standard (See Section 9).

5.1 LVDS (LOW VOLTAGE DIFFERENTIAL SIGNALING)

Low voltage differential signaling (LVDS) is a standard for communicating at high speed in point-to-point applications. LVDS uses differential signaling, a two-wire communication method where receivers detect data based on the voltage difference between two complementary electrical signals. This greatly improves noise immunity and minimizes emissions. It is a way to communicate data using a very low voltage swing (about 350 mV) over two differential PCB traces or a balanced cable.

5.1.1 TERMINATION

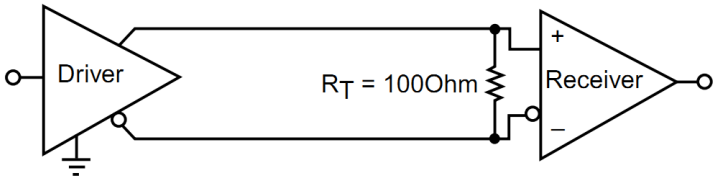


*Figure **16**: LVDS Point-to-Point Link*

LVDS technology can be used with distance ranging from a few inches to 10 meters

To prevent reflections, LVDS requires a terminating resistor of 100 Ω ± 20 Ω that is matched to the actual cable or PCB traces. This resistor completes the current loop and properly terminates the signal. This resistor is

[18] http://www.eetimes.com/document.asp?doc_id=1272339

placed across the differential signal lines as close as possible to the receiver input. With this termination, an LVDS driver (DS90C031) can drive a twisted pair wire (e.g., SCSI cable) over 10 m at speeds in excess of 155.5 Mbps (77.7 MHz).

5.1.2 DATA RATE AND CABLE LENGTH

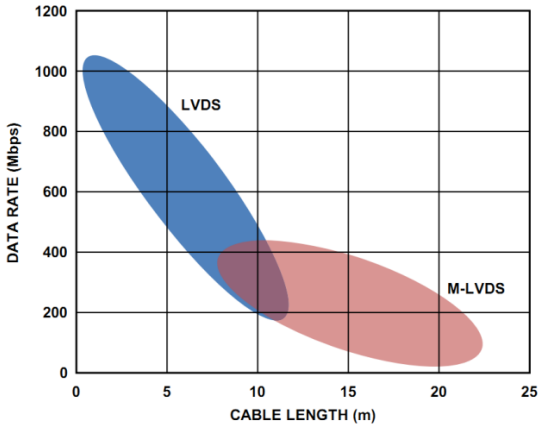


*Figure **17**: Cable Length (Twisted-Pair) vs. Data Rate for Some Typical LVDS and also M-LVDS[19] applications*

LVDS is currently one of the fastest low power data transmissions available. As the demand for higher rate increases, LVDS will become more crucial.

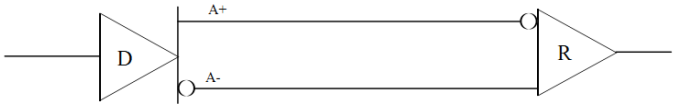
5.2 RS422

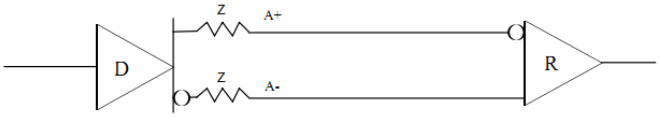
The RS-422 standard specifies data rates up to 10 Mbps and line lengths of up to 4000 feet and if termination is to be used it must be placed at the end of the cable near the last receiver.

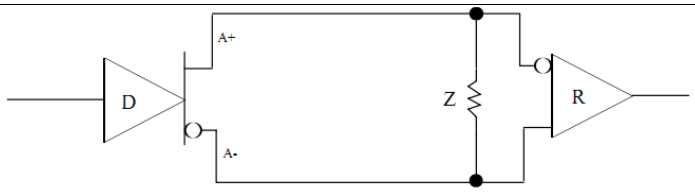
In general, RS-422 driver outputs (See A+ and A- in Termination section) should not exceed ±6 V with respect to ground. The differential voltage between them should be greater than ±2 V but not exceeding ±10 V. By the time the signal pair reaches the receiver, the differential voltage must be greater in magnitude than 200 mV (input sensitivity) to get valid state changes.

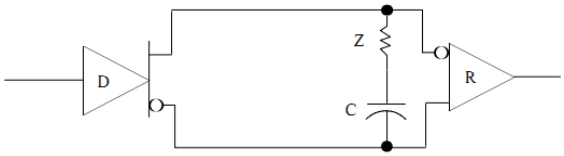
[19] Multi-Drop LVDS

5.2.1 TERMINATION

<table>
<tr><th>No Termination</th><th>Series Termination</th></tr>
<tr><td> 

The input resistance of the receiver, as defined by the 422 standard, will be around 4 kΩ. Under these conditions, there will be some signal reflection at the receiver end but it should not be large enough to produce invalid data.</td><td> 

The resistors are chosen such that their value, plus the driver’s output impedance matches the transmission line’s characteristic impedance. Like the no termination example, a reflection will still be generated at the receiver end but will encounter proper termination once it gets back to the driver eliminating any additional reflections. As a result, data rates will still need to stay low. In addition to signal reflection, another major disadvantage is that series termination is only appropriate for point-to-point applications.</td></tr>
<tr><th>Parallel Termination</th><th>AC termination</th></tr>
<tr><td> 

By far the most widely used termination method, parallel termination consists of a single resistor connected across the differential inputs at the receiver. The resistor value “Z” is chosen to match the characteristic impedance of the cable as best as possible (±20%). This will, in effect, make the cable appear purely resistive eliminating signal reflections. This technique supports higher data rates and longer cable runs but will increase the driver’s power draw due to the current now passing through this resistor.</td><td> 

If both power consumption and signal quality are major concerns, AC Termination offers a compromise between the parallel, series and unterminated schemes. By adding a capacitor in series to the termination resistor the DC current draw is significantly reduced while still keeping signal reflections low.

During a state change, the capacitor acts like a short making the termination appear to be like the parallel example. During steady state, the capacitor charges up and acts like an open making the line appear unterminated. The main disadvantage of this technique is the reduction of data transmission rates due to the resulting RC time constant. The capacitance “C” should be chosen so that the resulting RC time constant is low with respect to the unit interval. Consider the following example:</td></tr>
</table>

AC termination example:

Suppose we use a multiple twisted pair cable (Belden 9831) with a characteristic impedance of 100 Ω and a nominal propagation delay of 1.6 ns/ft. To choose the appropriate value for C, use the following equation:

C≤ (round trip cable delay/characteristic impedance)

For a cable 100 ft long, we get C ≤ 3,200 pF [100 ft x 2 x 1.6 ns/ft/ 100 Ω].

For a cable only 20 ft long, the same equation yields a value of C ≤ 640 pF.

In addition to this, use the following rule-of-thumb for choosing a maximum data rate:

RC time constant ≤ 10% of unit interval

Working the 100 ft example backwards yields a switching rate that should not exceed 312.5 kHz.

Termination	Signal Quality	Data Speed	Power Dissipation
No Termination	Poor	Low	Low
Series	Good	Low	Low
Parallel	Excellent	High	High
AC	Good	Mid-range	Mid-range

Table 3: termination techniques quick comparison

5.2.2 DATA RATE AND CABLE LENGTH

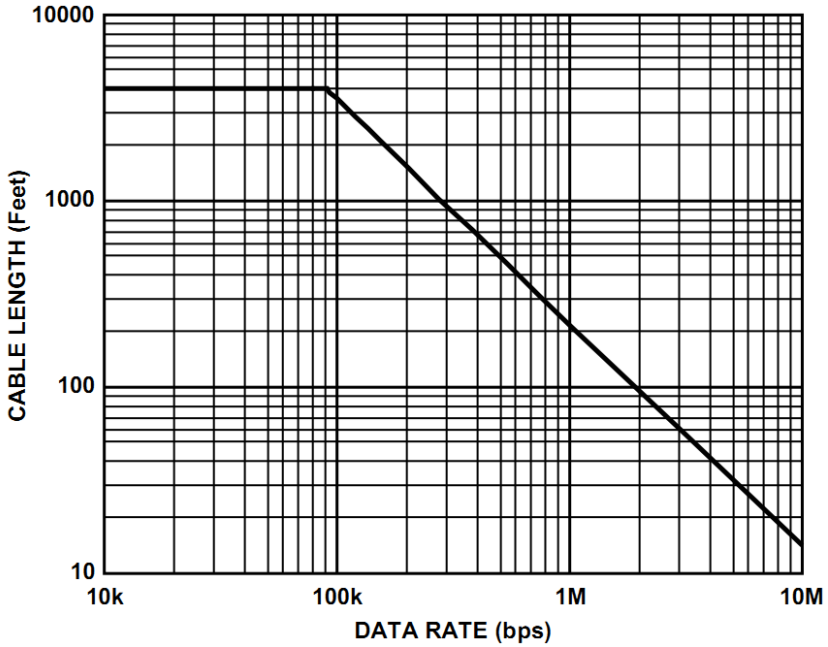


*Figure **18**: Cable Length vs. Data Rate*[20]

Examples of data rate and cable length combinations vary from 90 kbps at 4000 feet to 10 Mbps at 15 feet for RS-422.

5.3 A QUICK COMPARISON:

Parameter	RS-422	LVDS
Differential Driver Output Voltage	±2-5 V	±250-450 mV
Receiver Input Threshold	±200 mV	±100 mV
Data Rate	< 30 Mbps	> 400 Mbps

[20] http://www.analog.com/static/imported-files/application_notes/AN-960.pdf

6. ALTERNATIVES WHEN SYSTEM-TO-SYSTEM REQUIRES HIGHER VOLTAGE

OPAL-RT provides DIO that can transmit signal from 5V to 30 V, based on a type B board 32Dout **Push_pull**.

32 isolated DOUT Push-Pull	
OP5360-1	OP5360-2
Wide operating voltage range:	
▪ from Vuser=5VDC up to 15VDC max	▪ from Vuser=5VDC up to 30VDC max
Output Current rating	
Max: 50 mA / Channel [before trip action] Outputs may be connected in parallel for higher (2 times) current capability, ▪ Use matched pairs like DOUT_0 & 1, DOUT_2 & 3…	
Propagation delay (In/Out)	
≤ 50 ns @ 25 °C	≤ 200 ns @ 25 °C at 5 V ≤ 65 ns @ 25 °C from 15 to 30 V
Rise/Fall times	
≤ 15 ns	≤ 15 ns
Operating frequency	
DC-500 kHz	
Output configuration	
Not Tri-Stated ➔Forced to a low state, when undriven, unpowered or when OV protection is reached.	Tri-state when undriven, unpowered or when OV protection is reached

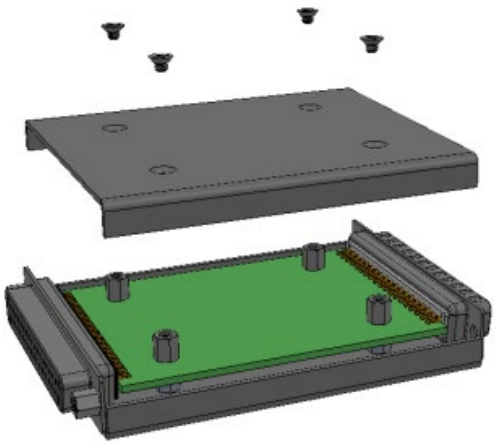
Recommendations:

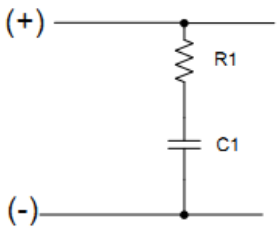
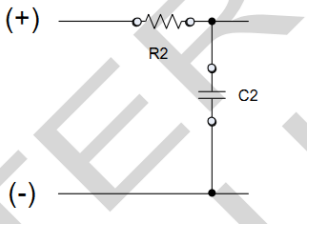
- Users should adjust the power supply level (through the DB37 connector Pin 18: Vuser and Pin 37: Vuser_RTN) to get the proper high voltage level at the DOUT.

- Use a proper damping circuit (a serial resistor capacitor circuit tied to the GND as close as possible the user **D**evice **U**nder **T**est, DUT) to minimize ringing and over/undershoot according to the connection length (from OP5360-1 to user DUT).
    - The following parameters are a good starting point for the RC values:
      R=150Ω, C = 100 pF. Tuning is necessary, according to application parameters.

Accessories:

To adjust the signal integrity, Opal provides two different DB37-to-DB37 boards:



OP8320-1	OP8320-2
126-496_DB37_to_DB37_Signal_Protection_Snubber	126-0498_DB37_to_DB37_RC_Filter
SNUBBER FILTER 	**RC/LC FILTER** 

7. CONCLUSIONS

The document has presented the TTL and CMOS characteristics, how to interface TTL and CMOS logic devices and five techniques to terminate the lines, so the signal quality is maintained (ringing, over/undershoots can cause false triggering, stair stepping, delays and loss of noise margin).

It has also been addressed two different approaches to assess whether or not to terminate a line.

OPAL-RT recommend not to exceed 1.5 m with the DIO TTL/CMOS boards to interconnect CMOS/TTL driver / receiver on different chassis or equipment.

If a system-to-system requires:

- A longer distance to transmit data, OPAL-RT recommend to use a differential signal transmitting standard, as LVDS or RS422. OPAL-RT provides 32×DIO boards either for LVDS @ 3V3 or RS422 in a 3V3 or 5V version,
- Higher voltage, from 5V to 30 V, OPAL-RT can also offer isolated solutions in 32×DIO boards.

More specifically, this document intends to warn of possible signal distortions / degradations when no precaution has been taken into account such as excessive cable length, improper terminations, too much capacitive cables, or high signal frequency… To keep a good signal integrity requires, well-informed users able to adapt the lines.

To wrap –up,

OPAL-RT has purposely designed a prototype DB37 to DB37 board (OP8320-4) to help users terminate the lines when facing signal distortion while using the TTL/CMOS boards (126-0429 & 126-0430). It provides the possibility to use one of five methods discussed in this paper,

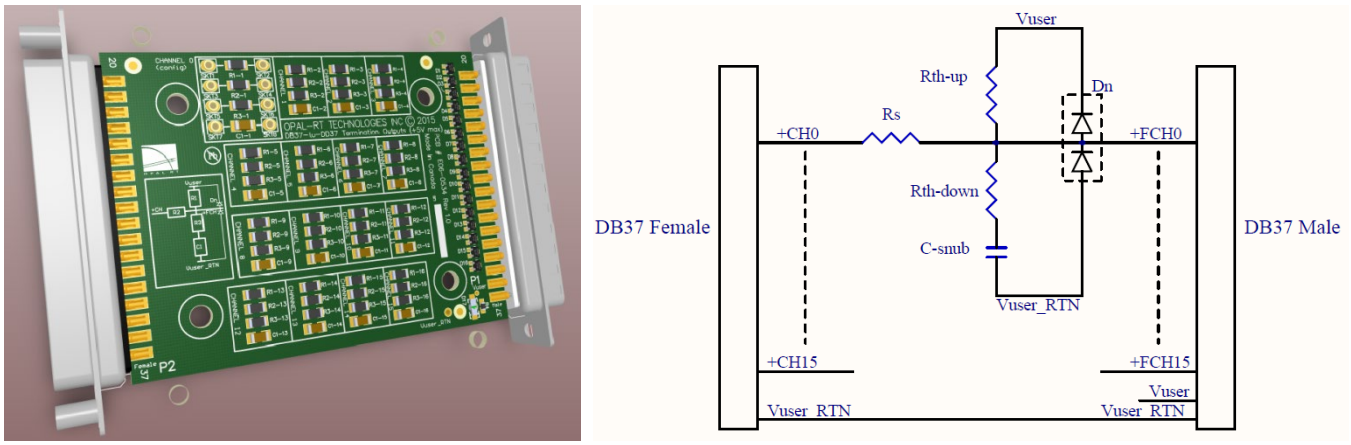


*Figure **19**: DB37 to DB37 termination_outputs*

8. REFERENCES

[1] H. Johnson and M. Graham, High-Speed Digital Design. Upper Saddle River, NJ: Prentice Hall, pp.2, 166-167.

9. OPAL-RT DIO BOARD LIST

- OP5351 32DIN_TTL_TypeB (Configurable 5 V or 3V3)
- OP5352 32DOUT_TTL Type B (Configurable 5 V or 3V3)
- OP5354 Opto-Isolated 32DOUT_Push-Pull_TypeB (obsolete)
- OP5355-3 Opto 32_Dout_LVDS_3V_TypeB
- OP5356-5 Opto 32_Dout_RS422_5V_TypeB
- OP5356-3 Opto_32_Dout_RS422_3V_TypeB
- OP5357-3 Opto_32_Din_LVDS_3V_TypeB
- OP5358-5 Opto_32_Din_RS422_5V_TypeB
- OP5358-3 Opto_32_Din_RS422_3V_TypeB
- OP5360-1 Opto-Isolated 32 Dout Push-Pull FET Vuser: 5V to 15 V, delay In/Out 50 ns
- OP5360-2 Opto-Isolated 32 Dout Push-Pull FET Vuser: 15 V to 30 V, delay In/Out from 200 ns to 50 ns
- OP5363 32Din_High Impedance_TypeB [configurable IN/out by 8]
- OP5366 32 Single Ended Configurable Type B
- OP5367-1 32 bits Digital Out
- OP5367-3 16 bits Digital In, 16 bit Digital Out
- OP5367-5 32 bits Digital In

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