Warning: we are working on updating this manual to correspond to the new Windows interface

11.1 RECTIFIER/INVERTER 6/12 PULSE DC CONTROLLERS

11.1.1 Introduction

The HVDC converter library contains both 12-pulse and 6-pulse models. The control system is the same for both types of converters. However, 12-pulse models offer the possibility of choosing between two types of synchronization systems. Since each converter can be operated as a rectifier or as an inverter, the set of parameters is the same for all four converter models. However, different icons and elements are provided to differentiate rectifiers and inverters. The control system[1] includes regulation, synchronization, protection and tap changer subsystems. The models can simulate a valve short-circuit or a DC fault. Step responses can also be simulated to optimize the regulator parameters. Finally, the thyristor bridge can receive firing pulses from four different sources:

- The internal generic control system provided with the converter;
- An external physical source;
- Simulink;
- The HYPERSIM® control module (control block)
- A GTO based two-level voltage-source converter (VSC) may be modeled by using the GTO+diode switch type in the six-pulse inverter shown in Figure 11 - 4. The model implementation includes a logic for the simultaneous switching (OFF or ON) of a diode with the switching of a GTO in accordance with the correct sequence. In this case, the “precision valve” option is not operational.

1.This control system is only intended for the thyristor based bridge.

11.1.2 Icons and diagrams

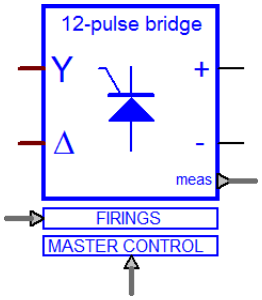


Figure 11 - 1 Icon and diagram of 12-pulse rectifier

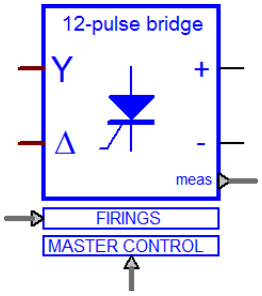


Figure 11 - 2 Icon and diagram of 12-pulse inverter

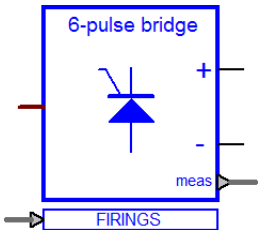


Figure 11 - 3 Icon and diagram of 6-pulse rectifier

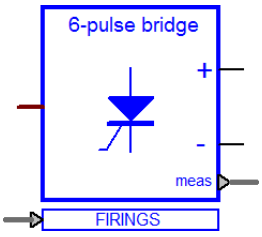


Figure 11 - 4 Icon and diagram of 6-pulse inverter

11.1.3 Modeling the converter and its control system

The general diagram of a converter station including a 12-pulse converter, a converter transformer and the generic control system is shown in Figure 11 - 5. For a 6-pulse converter, the bridge would be connected to one of the two secondary windings (star or triangle connections).

The general diagram of the control system is shown in Figure 11 - 6.

11.1.4 Valve faults and DC fault

It is possible to simulate a short circuit on any of the 12 valves (at the user's choice) for a specified time interval (see form in Figure 11 - 16). A resistive grounded DC fault can also be simulated at the converter terminal. The time interval is referenced with respect to the start of the acquisition, or t = 0.

11.1.5 Firing and synchronization system

The lag angle reference (a) is a firing system input. It is generated by the regulation system and the AC voltages of the switching bus. The synchronization system generates firing pulses for each thyristor. The generic synchronization system used in a 6-pulse converter is of the "equiangular" type. It can be used with a 12-pulse converter for which the user also has the option of using an "equidistant" synchronization system.

A – Equiangular synchronization mode

The firing pulses are synchronized with the zero crossings of the switching voltages.

B – Equidistant synchronization mode

The firing pulses are synchronized with an oscillator whose frequency is 12 times that of the power grid. The oscillator phase is controlled by the regulation system (current, voltage, etc.) which lags or leads the firing, if necessary. The oscillator synchronizes itself slowly at the zero crossings of the switching voltages, but quickly at the previous firing instant. The oscillator gain, set by the user, allows users to determine the speed at which the oscillator synchronizes itself with the zero crossings. A gain of 1 (minimum allowed) means a full synchronization with the zero crossings[1]. As the gain increases, the oscillator synchronizes itself more slowly with the zero crossings (1000 is the maximum limit imposed by the model). Hence, the system is not greatly affected by transients and unbalances of the AC switching voltages. A gain of 32 (default value) is a good compromise between the synchronization speed and the immunity to the harmonics on the switching voltages. In transient state or during AC faults, when the switching voltages are absent or severely distorted, the oscillator gain is automatically increased to cancel any zero crossing synchronization.

Note that a valve will be fired (pulse generated) only when the voltage at its terminals has reached a minimum threshold, adjustable by the user.

1.As it is the case for the equiangular synchronization system

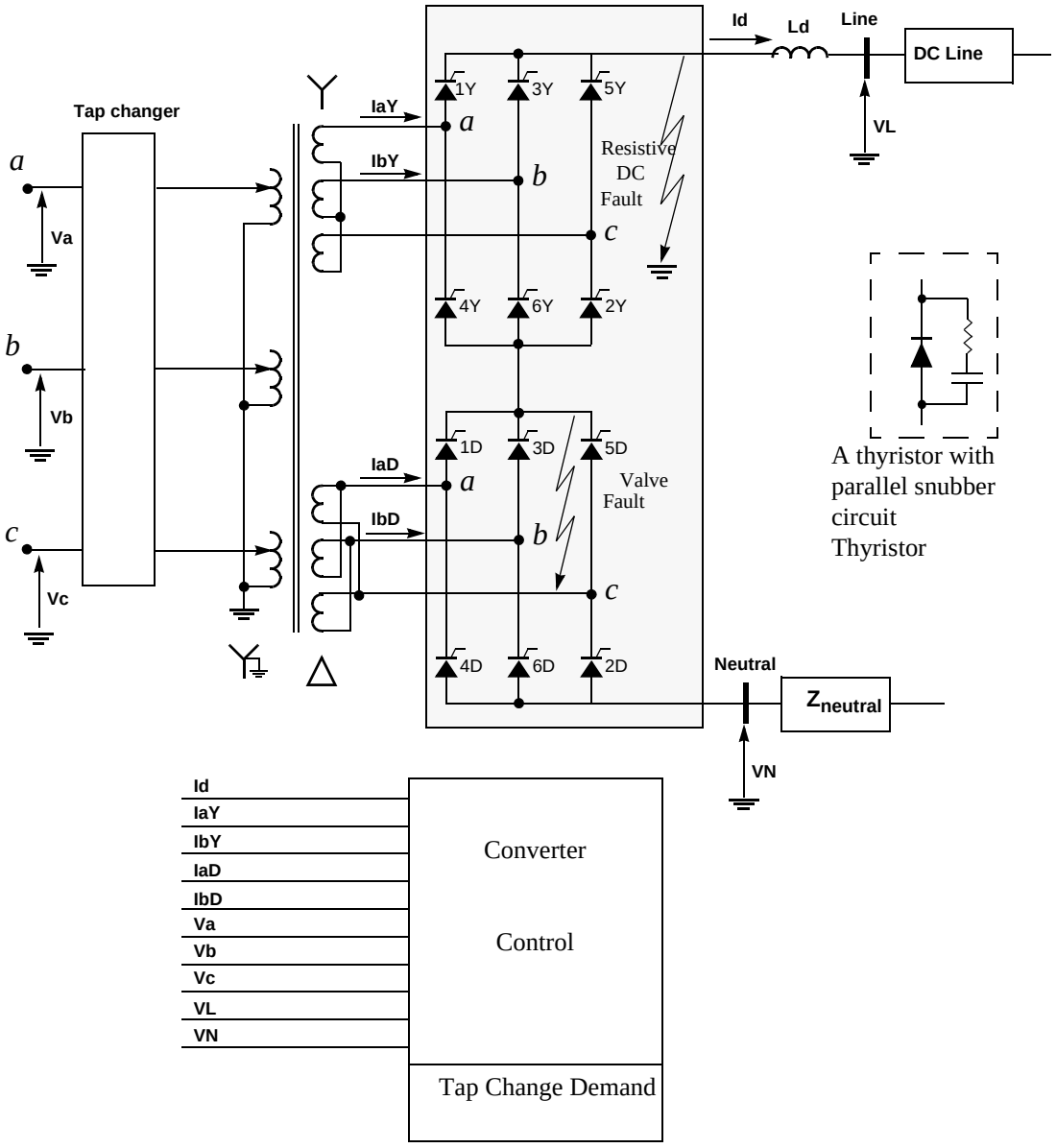


Figure 11 - 5 The general diagram of a 12-pulse converter bridge

11.1.6 Band-pass filter

The voltages used for synchronization are filtered by band-pass filters with an adjustable tuning frequency. The transfer function of one band-pass filter is:

$$H(s) = \frac{Bs}{s^2 + Bs + \omega_o^2} \qquad \text{(EQ 1)}$$

$$\omega_o = 2\pi f_o \qquad \text{(EQ 2)}$$

where

B Bandwidth in radians/second

ω_o Central pulsation in radians/second

f_o Central frequency (hertz)

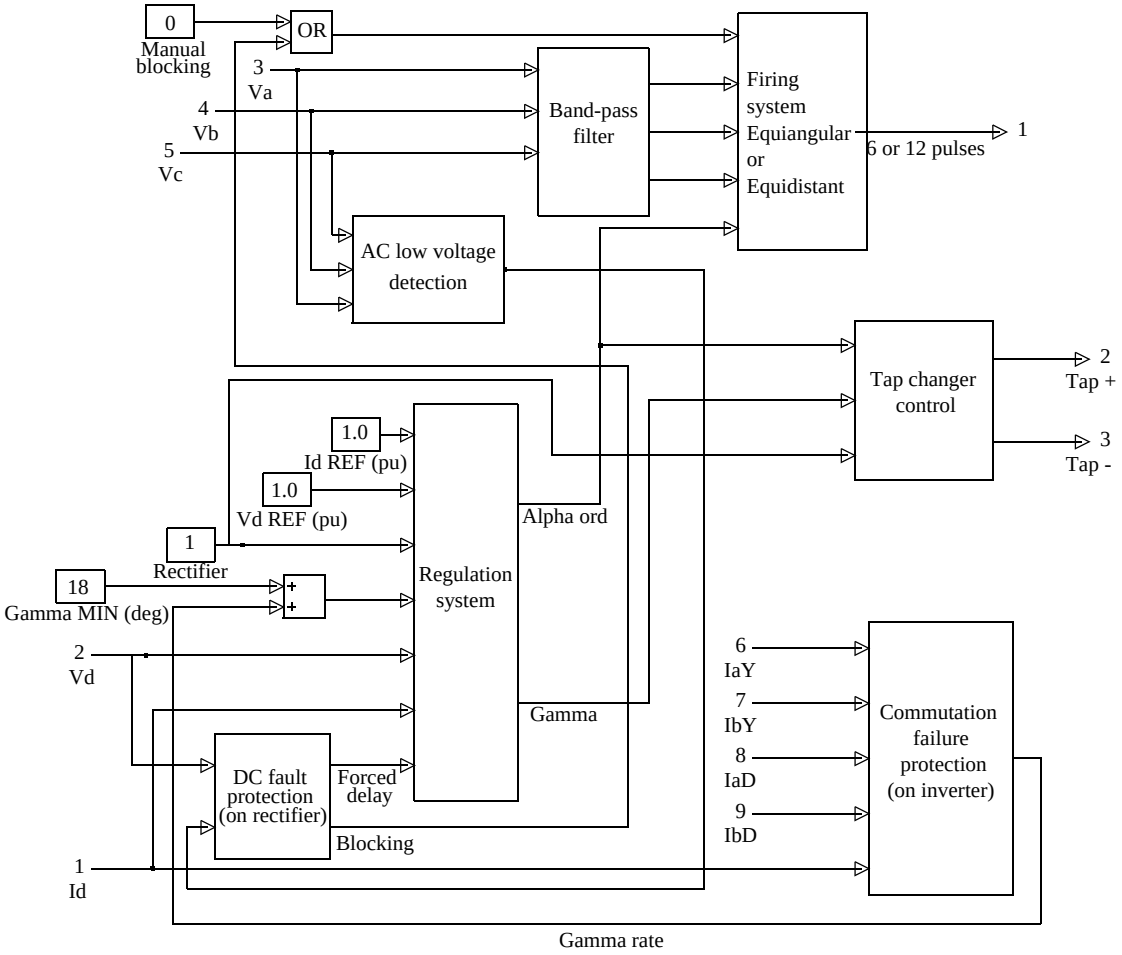


Figure 11 - 6 The general diagram of the generic converter control system

At f_o frequency, H(s) has a gain of 1 and its phase is zero. As a result, the band-pass filter does not affect the fundamental component of the voltage (neither in amplitude nor in phase), while it reduces other harmonic components.

The *B* parameter (proportional to the pass-band with a typical value of 45 Hz) is used to control the sensitivity and the speed of the filter. A small bandwidth improves harmonic filtering and gives less distorted wave-form at the filter output. However, the smaller the bandwidth, the slower the filter is in following the amplitude and phase fluctuations of the input signals.

The three-phase voltages on the primary side of the transformer are thus filtered by an adaptive band-pass filter. The six secondary (Y and Δ side) line voltages (phase to phase) calculated from the primary voltages are used to determine the zero crossing times. For each voltage, there are two zero crossings in one cycle, one with an positive slope and another with a negative slope for a total of 12 zero crossings in each cycle.

The period *T* is updated 12 times per cycle. The measured period T is limited within an adjustable interval defined by the Freq max and Freq min parameters.

11.1.7 Low AC voltage detection

If the voltage is lower than a specified threshold during a specified time interval, the "*Low AC voltage detection*" function provides a *low voltage* flag. In the equiangular synchronization mode this flag is on and the calculated period T is not updated. It is rather maintained at its past value in prevision of an eventual AC fault. Also, the DC fault detection is inhibited. A falling edge delay (from True to False) is applied to the flag to ensure that it remains present for a minimum period of time. Finally, low voltage detection is used in the "*DC fault protection*" described further ahead.

11.1.8 The α angle regulation and limiting system

The function of the regulation system is to regulate the direct current or voltage by adjusting firing angle α, and to limit the inverter extinction angle to a minimum value.

11.1.9 The static characteristic

The Vd-Id static characteristic of a rectifier-inverter system is shown in Figure 11 - 7.

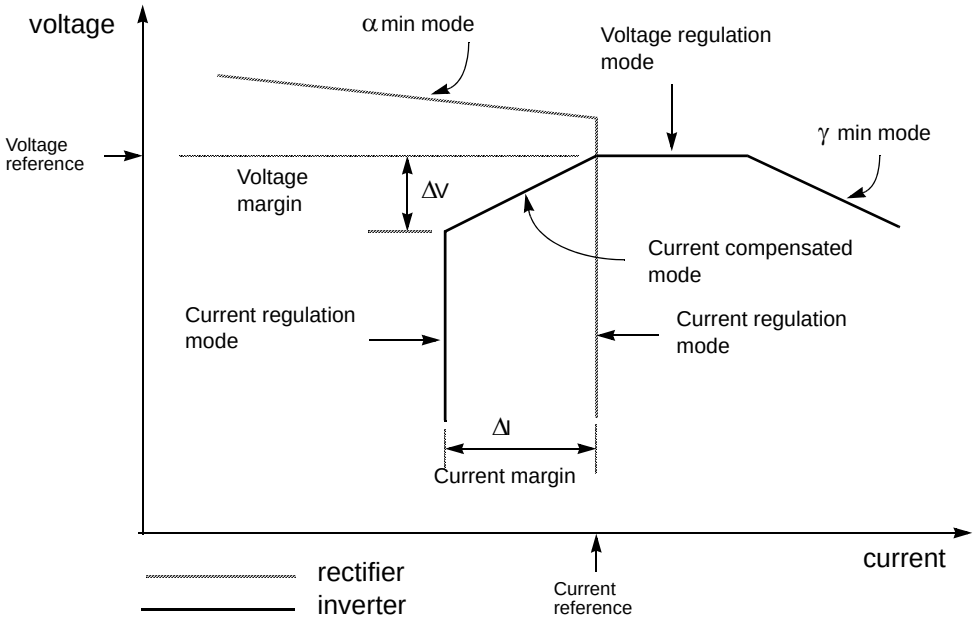


Figure 11 - 7 Vd-Id static characteristic

Normally, the rectifier regulates the direct current to maintain it equal to the current reference. In abnormal cases (e.g. voltage drop in the AC power system) the α delay angle can reach its minimal value α_{min} and the rectifier will not be able to regulate the current. In such a case, it is said to operate in "α_{min}" mode.

The inverter regulates the direct voltage *Vd* measured at the DC line input to keep it equal to the *voltage reference*. In Figure 11 - 7, the inverter operates in voltage regulation mode. If the current drops below the current reference, the inverter goes in "current *compensated mode*" where the voltage is regulated with a slope determined by the voltage margin (ΔV) and the current margin (ΔI). If the current falls even lower than the (current reference - current margin), the inverter will operate in "current regulation mode".

If the DC current increases (load increase or fault in the AC power system on the inverter side), the extinction angle γ can reach the minimal value allowed and the inverter can loose its regulating capability. It then operates in "γ_{min} mode".

11.1.10 The voltage dependent current order limiter (VDCOL)

Figure 11 - 8 shows the operation of the voltage dependent current order limiter. The object of this limiter is to ensure a good recovery of the DC power transit following faults on the AC side. The risk of commutation failure during recovery is also minimized.

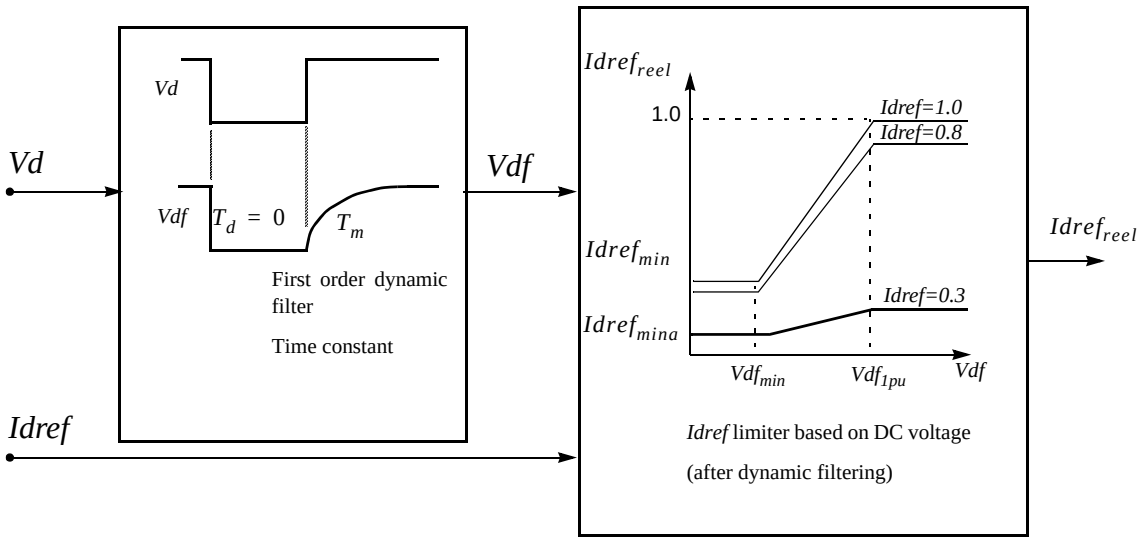


Figure 11 - 8 Voltage dependent current order limiter (VDCOL)

The limiter includes two functions: the dynamic filtering of the DC voltage and the calculation of the reference based on the filtered voltage.

1 Dynamic filtering of the voltage – The DC voltage *Vd* goes through a first order filter whose time constant *T* varies:

- $T = T_d = 0$ when *Vd* decreases;
- $T = T_m = 80ms$ when *Vd* increases.

In this way, the current reference falls immediately when the voltage drops, but increases more slowly when the voltage rises. This allows for quick but controlled recovery of the direct power transit.

The typical values of the following adjustable parameters are:

$Idref_{min}$ = 0,3 p.u.
Vdf_{min} = 0,18 p.u.
Vdf_{1pu} = 0,6 p.u.
$Idref_{mina}$ = 0,1 p.u.

11.1.11 Dynamic operation of the controller

The functional diagram of the controller is shown in Figure 11 - 9. This pole control function is the same for the rectifier and the inverter.

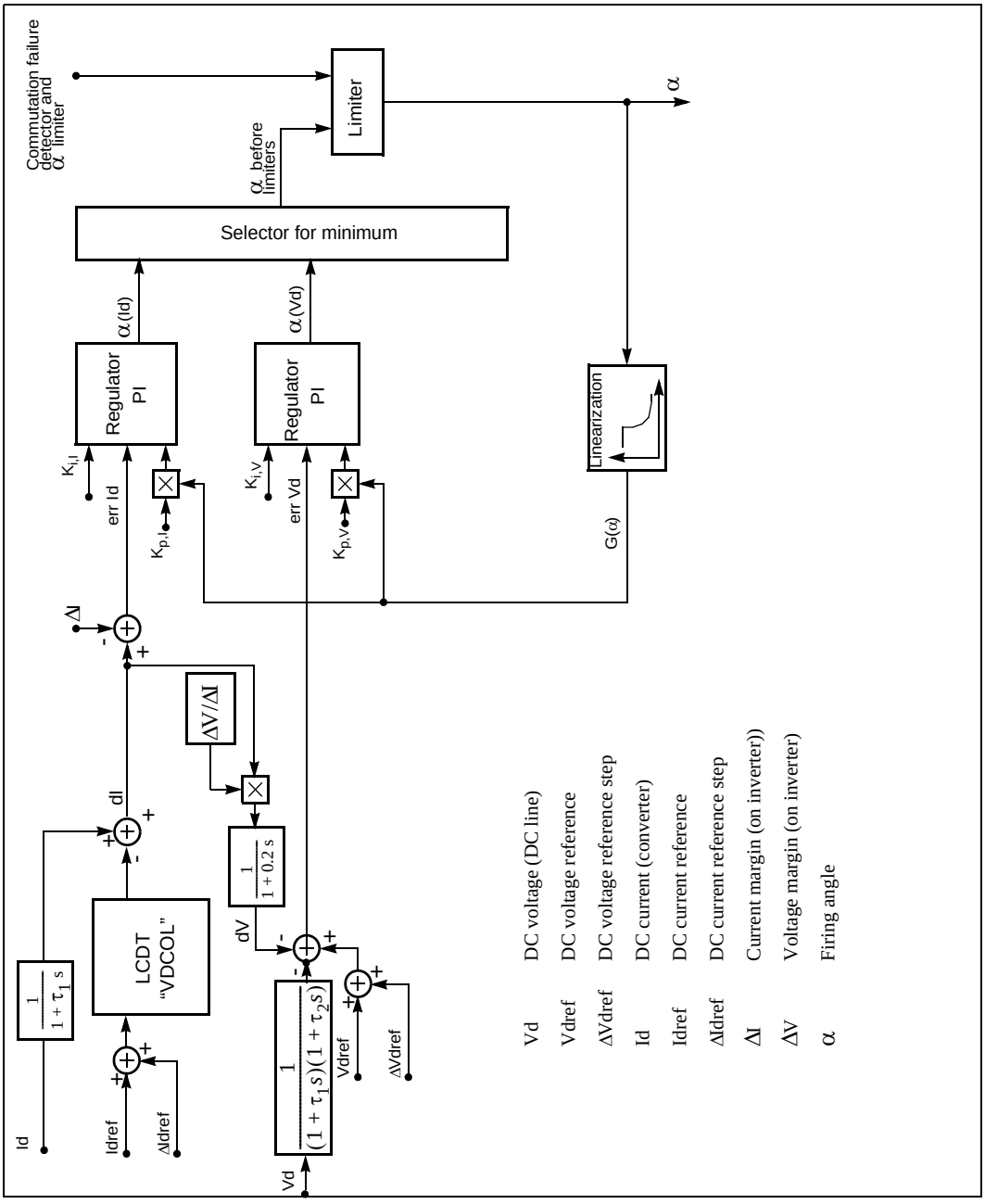


Figure 11 - 9 Functional diagram of the regulation unit

The regulation unit essentially consists of two PI (proportional-integral) regulators with limiters: one for the current and the other for the voltage. The delay angle α is established by the lowest value among the outputs of the two regulators.

On the rectifier side, the reference current *Idref* takes on a normal value (e.g. < 1.2 p.u.) while the voltage reference *Vdref* takes on a very high value (e.g. 2 p.u.). In this way, the regulation unit cannot regulate the voltage and will be forced to operate in current regulation mode. A signal allows users to apply a current reference step for a specified time interval.

On the inverter side, a current margin ΔI is subtracted from the inverter reference, usually equal to that of the rectifier, so that in normal state, there is a ΔI error at the PI input. The inverter regulates the voltage at the DC line input.

11.1.12 The PI regulators

The PI regulator includes the following transfer function:

$$H(s) = K_i\left(\frac{1}{s} + T_p G(\alpha)\right) = \frac{K_i}{s} + K_i T_p G(\alpha) \qquad \text{(EQ 3)}$$

where

K_i is the integral gain;

$K_i T_p = K_p$ is the proportional gain;

$G(\alpha)$ is the linearization factor (see Figure 11 - 10).

Upper and lower limits are applied to the regulator output (representing the α delay angle) to ensure it remains within safe range of operation.

11.1.13 Linearization of gain

The linearization is done by multiplying the proportional gain by a factor $G(\alpha)$ depending on α as shown in Figure 11 - 10.

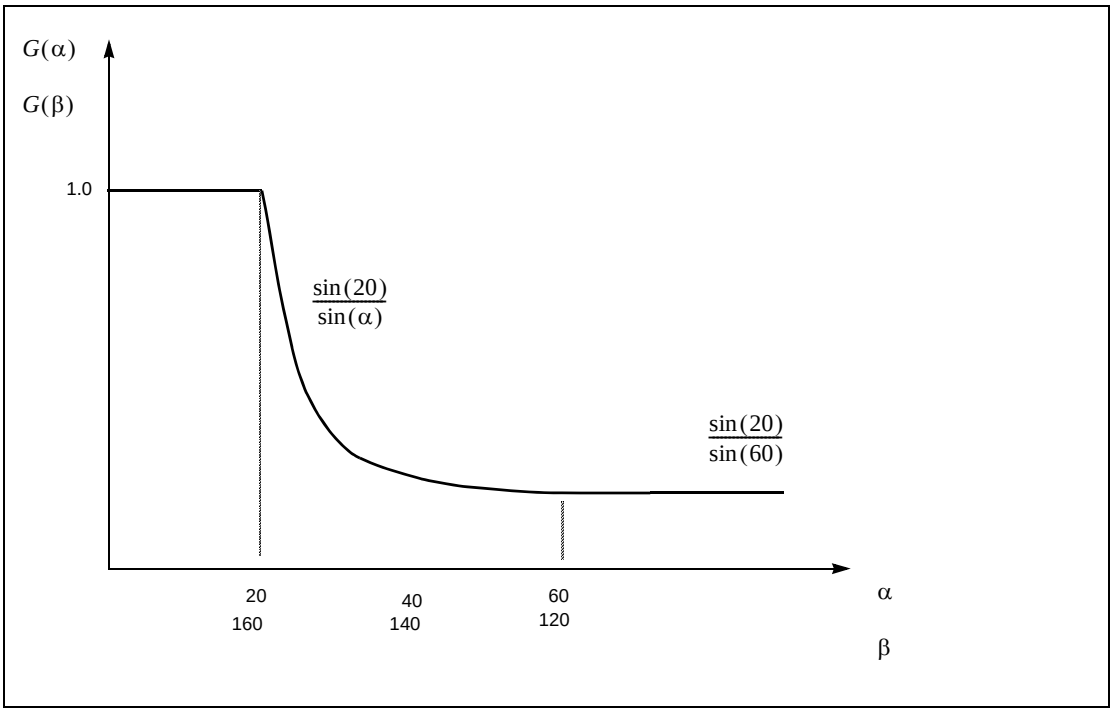


Figure 11 - 10 Correction factor for proportional gain of PI regulators

This linearization is necessary to have the regulation respond with the same speed at different values of α.

On the inverter side, the linearization is applied on the $\beta = 180° - \alpha$ and G(β) looks the same as G(α).

The linearization of the gain does not apply to the integral part of the PI regulator because this part of the response is slower.

The regulator output goes through two limiting functions before being sent to the firing unit. These functions are: α limiter and $\Delta\alpha$ limiter.

11.1.14 α limits

On the rectifier side, α is limited between two adjustable values. The typical limits are:

$$\alpha min_{rec} = 5^{o} \qquad \text{(EQ 4)}$$

$$\alpha max_{rec} = 168^{o} \quad \text{(EQ 5)}$$

Note : In the "equidistant mode" of the synchronization, the αmin_{rec} is not used.

On the inverter side, the lower limit is an adjustable constant, while the upper limit varies dynamically:

$$\alpha min_{inv} = 102^{o} \quad \text{(EQ 6)}$$

$$\alpha max_{inv} = 180 - (\gamma_{min} + \mu) - \gamma_{cf} \quad \text{(EQ 7)}$$

where

γ_{min} is the adjustable minimum value of the extinction angle

γ_{cf} is the adjustable reduction on αmax_{inv} when a commutation failure is detected (see Section 11.1.18**)** in order to reduce the risk of successive commutation failures.

μ is the calculated overlap angle

Note that

$$\gamma_{min} + \mu = \beta_{min} \quad \text{(EQ 8)}$$

11.1.15 ($\Delta\alpha$) limitation

In addition to the limit on the value of α, a limit is also imposed on the variation rate ($\Delta\alpha$) of α as shown in Figure 11 - 11. On the rectifier side, α is limited between two adjustable values. The typical values are:

Note that in the "equiangular" synchronization system, Da is the difference between the current reference and the previous firing reference. In an "equidistant" synchronization system, $\Delta\alpha$ is the difference between the reference "a" and a value of "a" reflecting the position of the oscillator phase (See section 11.1.5).

At the rectifier and the inverter, $\Delta\alpha$ is within a value range where only the vertical coordinates are adjustable. The typical values for the ordinates (X-axis) are: [Da1, Da2, Da3, Da4] = [90°, 5°, -10° and -5°] (rectifier); [Da1, Da2, Da3] = [6°, 1°, -6°] (inverter).

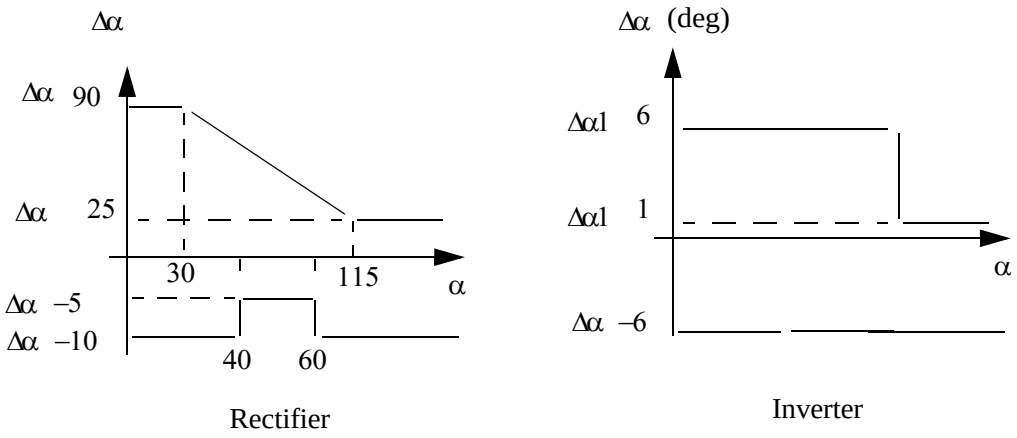


Figure 11 - 11 Limitation of Δα

The values marked in Figure 11 - 11 are for illustration only, they can be adapted to the dynamic characteristic of a particular network. The purpose of imposing limits on Δα is to:

- reduce the risk of commutation failure particularly when the value of α is high;
- improve the stability of the control system in case of faults or other large disturbances.

The side effect of limiting the variation rate of Δα is to slow down the response of the control system.

11.1.16 Protection system

Two protection functions are implemented in the control system: Protection for DC fault on the rectifier and Protection for commutation failure on the inverter.

11.1.17 DC fault protection

A fault in the DC power system is detected on the rectifier side when the following two conditions occur:

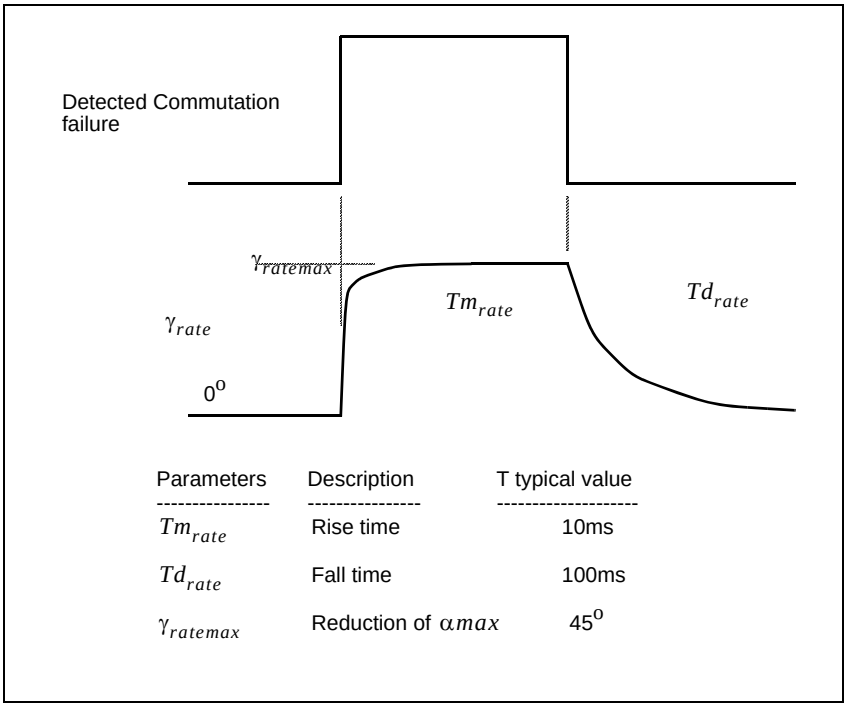
- The DC voltage falls below a specified threshold for a period of time (adjustable);
- No low AC voltage is detected on the rectifier side (characterizing a fault on the AC side). This detection is done in the *"Low AC voltage detection"* function described earlier.

When a fault is detected on the DC side, the rectifier α angle is forced to an adjustable value greater than 90^o so that the rectifier operates as an inverter to de-ionize the fault. This forced α is removed after an adjustable period of time. This operation will be repeated until the fault is cleared or the converter is blocked by the protection system after the operation has been repeated a number of times.

This function is implemented for simulating faults on the DC side. The function does not discriminate between the faults on the AC side of the inverter and commutation failures on the inverter, both causing a drop in direct voltage. One way to disable the protection is to assign a very large value to "detection time" parameter.

No action is taken on the inverter side since it is already in safe condition.

11.1.18 Protection for commutation failures



Parameters	Description	T typical value
Tm_{rate}	Rise time	10ms
Td_{rate}	Fall time	100ms
$\gamma_{ratemax}$	Reduction of αmax	45^o

Figure 11 - 12 Variation of γ_{cf} when detecting a commutation failure

The protection against commutation failure is provided on the inverter only. The reason is the firing angle on the inverter side is large and, therefore, the inverter is more prone to commutation failures.

The detection of commutation failures is based on the following principle. In normal state, the currents (in pu) on the AC side and on the DC side are nearly equal. A commutation failure instantaneously creates a short circuit on the DC side and the DC current increases quickly. The inverter then has a null voltage and hence, the current drops on the AC side. Therefore, a commutation failure is detected if:

- $Id - Iac > Tolerance$
- $Iac < Iac_{cf}$

with, $Tolerance = 0,15 + 0,1Id$ and $Iac_{comfail} = 0,65$ pu

When a commutation failure is detected, the protection decreases the upper limit of α by γ_{cf} as shown in equation (EQ 7). This keeps α away from the area where the risk of commutation failure is high. γ_{cf} then takes on the form shown in Figure 11 - 12: γ_{cf} increases quickly (adjustable first order time constant) when a commutation failure is detected for quick protection, but decreases more slowly (adjustable first order time constant) to avoid successive commutation failures.

It is possible to simulate commutation failures by preventing the current from switching from one thyristor to its neighbor. To do so, a given thyristor (1 of 12 as per user's choice) is prevented from receiving the firing pulse for a given period of time (adjustable).

11.1.19 Unblocking sequence

There are two ways to unblock the converters (e.g. following a persistent DC fault): manually or automatically.

Manual unblocking of a converter is initiated by the operator and takes effect only when the DC current is lower than a specified threshold (set at 0,10 p.u.). This current must then be decreased by lowering the current reference. All the reference signals have a rate of change limiter which limits their variation speed (adjustable).When the operator varies the reference, the effective reference will follow, but at a speed limited by the rate of change limiters.

The automatic disabling takes effect immediately to protect the system. It is controlled by the DC fault protection system.

When the converter is disabled (manually or automatically), the control system cancels the firing pulses to the valves. Moreover, a constant delay angle is imposed permanently.

11.1.20 Enabling (start-up)

Unblocking can only be done manually. To enable the converter, the user must:

- Set the current reference to zero;
- Initiate the enabling order. Regular pulses will be sent to the thyristors (instead of pulses from bypass thyristors).
- Set the current or voltage reference to the desired value. After unblocking, the converter will adjust to this given value with a certain delay depending on the limits imposed by the rate of change limiters. To maintain the current margin, the current ramp on the rectifier cannot be slower than that of the inverter at start-up.

11.1.21 The tap changer

The converter transformers (rectifier and inverter) can be equipped with a tap changer.

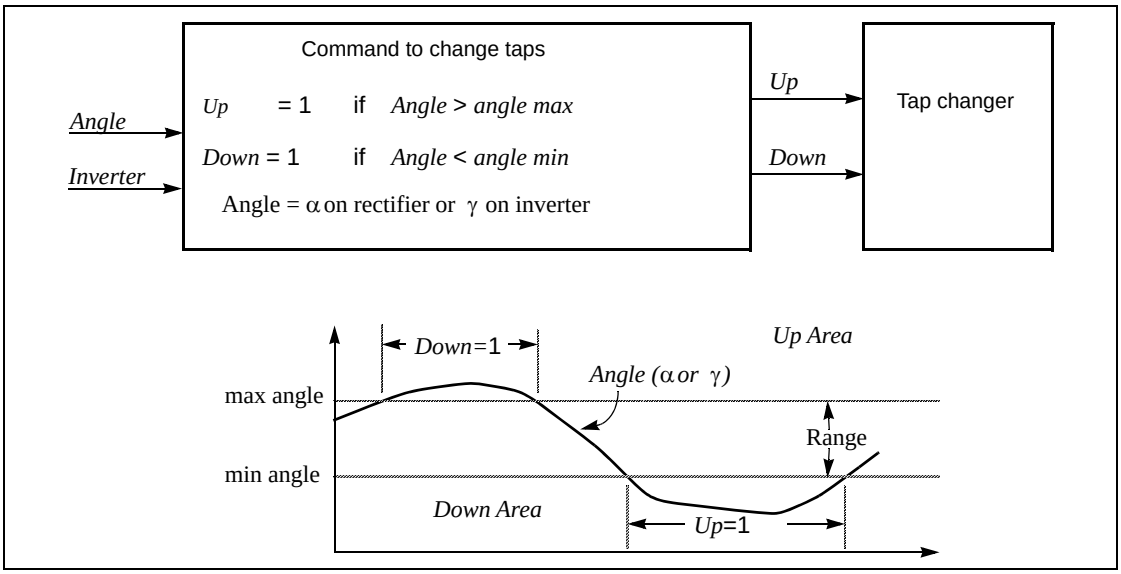


Figure 11 - 13 Demand to change taps

The tap changer controller generates the *Up* or *Down* order sent to the tap changer of the converter transformer in order to maintain α or γ angle in the range set by:

$$\alpha_{min} < \alpha < \alpha_{max} \quad \text{on the rectifier} \qquad \text{(EQ 9)}$$

$$\gamma_{min} < \gamma < \gamma_{max} \quad \text{on the inverter} \qquad \text{(EQ 10)}$$

If the angle is not within the range, an up or down request is generated and sent to the tap changer in order to bring the angle back within the range (if the tap has not yet reached any of the limits). The size of the range must be selected to avoid hunting (i.e. oscillation of the angle between the *Up* area and the *Down* area). Usually:

Range = at least 1.5 x maximum variation of angle corresponding to a tap

The default range values (adjustable) are shown in the following table.

Table 1: Typical angles limiting the range

Angle	*Min Angle*	*Max Angle*
α	15°	18°
γ	17°	20°

11.1.22 Description of parameters

The parameter form of HVDC converters are shown in Figures 11 - 14 to 11 - 17

11.1.23 References

- Id Ref: Current reference (pu);
- Id Ref + Slope: Current reference rising rate (pu/s);
- Id Ref - Slope: Current reference falling rate (pu/s);
- Id Ref min: Current reference lower limit (pu);
- Id Ref max: Current reference upper limit (pu);
- Vd Ref: Voltage reference (pu);
- Vd Ref + Slope: Voltage reference rising rate (pu/s);
- Vd Ref - Slope: Voltage reference falling rate (pu/s);
- Vd Ref min: Voltage reference lower limit (pu);
- Vd Ref max: Voltage reference upper limit (pu).

11.1.24 Converter parameters

- General parameters
  - Vd Base: Base for direct voltage (kV);
  - Id Base: Base for direct current (kA);
  - Vac Base (Ph-Ph): Rated AC voltage on the transformer primary (kV rms);
  - Synchro Bus: Name of the bus whose voltages are used to synchronize the firing system;
  - Line Bus (Vd Measure): Name of the bus connecting the converter and the DC line; the direct voltage measurement is taken on this bus;
- Converter transformer
  - Transfo name: Transformer label;
  - Leakage: Leakage inductance of converter transformer for star or delta winding on valve side (henry);

Note : Used to determine the commutation resistance to calculate the γ and μ angles. It is assumed that the leakage on the primary side is null and that no series inductance is connected between the switching bus and the transformer. Otherwise, the primary leakages and/or series inductance will be brought back on the secondary side and included in the leakage L.

  - Δ/ Y (lagging = 0, leading = 1): Indicates the relative phase between secondary windings of the transformer. If “0”, the delta winding lags the wye winding; if “1”, the delta winding leads the wye winding.

11.1.25 Operating modes

- Converter mode (rectifier = 0, inverter = 1): Operating mode of the converter;

- Blocking (Disabled = 0, Enabled = 1): If “0”, the converter is disabled; if “1” the converter is enabled;
- Regulator mode α constant IN/OUT(0/1): “1” for constant α regulation mode, “0” for normal mode;
- α constant reference: Value of the delay angle α when operating in constant α mode (degrees).
- Cathode connection (Neutral = 0, Line = 1): Specifies where the cathode side of the converter is connected; neutral side or DC line side.
- Firing (internal = 0; external = 1)

11.1.26 Controller parameters

- Firing (0 = internal, 1 = external, Simulink=2, Control Block=3): Specifies the source of firing pulses;
- Simulink:
  - Model name: Name of the Simulink model;
  - Model directory: Name of the directory in which the Simulink model is stored;
  - Execution time: Estimated or measured execution time of the Simulink model.
- UCC command: Always disable (not yet supported).
- As a Rectifier
  - KI Id: Integral gain of the PI current regulator (degrees/pu/second);
  - KP Id: Proportional gain of the PI current regulator (degrees/pu/second);
  - α_{min}: Lower limit of the delay angle α (degrees);
  - α_{max}: Upper limit of the delay angle α (degrees).
  - $\Delta\alpha 1$, $\Delta\alpha 2$: Limit values for the positive variation of delay angle α (degrees)) (See Figure 11-11);
  - $\Delta\alpha 3$, $\Delta\alpha 4$: Limit values for the negative variation of delay angle α (degrees) (See Figure 11-11);
- As an inverter
  - KI Id: Integral gain of the PI current regulator (degrees/pu);
  - KP Id: Proportional gain of the PI current regulator (degrees/pu);
  - KI Vd: Integral gain of the PI voltage regulator (degrees/pu);
  - KP Vd: Proportional gain of the PI voltage regulator (degrees/pu);
  - γ_{min}: Lower limit for the γ angle (degrees);
  - α_{min}: Lower limit for the α angle (degrees);
  - Id Margin: Current margin (pu);
  - Vd Margin: Voltage margin (pu);

  - $\Delta\alpha 1$, $\Delta\alpha 2$: Limit values for the positive variation of delay angle α (degrees) (See Figure 11-11);
  - $\Delta\alpha 3$: Limit value for the negative variation of delay angle α (degrees) (See Figure 11-11);
- Synchronization system at firing:
  - Synchronization mode (Equidistant, Equiangular): “Equidistant” for equidistant synchronization mode; “Equiangular” for equiangular synchronization mode.
  - Vmin: Minimum voltage value at valve terminal, so that the equidistant synchronization mode can fire the valve (pu).
  - K osc: Oscillator gain.
  - Tap changer transformer with decoupling element: “Enabled”, “Disabled”.
  - Transformation ratio, in the event that this last transformer is not used: “Ratio”, where 1.0 (pu) represents the rated ratio Ns/Np.

11.1.27 Measurement filters

- First order for Id ($\tau 1$): Time constant of the filter used in the current measurement (seconds);
- Second order for Vd ($\tau 1$, $\tau 2$): Time constants of the filter used in voltage measurement (Seconds);

11.1.28 Band-pass filters (Synchronization)

- Freq base: Frequency base (hertz);
- Freq min: Lower limit of acceptable frequency (hertz);
- Freq max: Upper limit of acceptable frequency (hertz);
- Band-pass: Bandwidth of the filter (hertz);

11.1.29 LCDT <<VDCOL>> function

- Vd min= Vdf_{min} in Figure 11 - 8;
- Id min= $Idref_{min}$ in Figure 11 - 8;
- Rise time= T_m in Figure 11 - 8;
- Vd threshold= Vdf_{1pu} in Figure 11 - 8;

Note : When the user changes the reference, the effective reference varies from the previous value to the requested value following a ramp whose slope is adjustable in both directions (rise and fall).

11.1.30 Tap changer control

(see Figure 11 - 13)

- α_{min}: Lower limit of alpha angle range on rectifier (degrees);
- α_{max}: Upper limit of alpha angle range on rectifier (degrees);
- γ_{min}: Lower limit of gamma angle range on inverter (degrees);
- γ_{max}: Upper limit of gamma angle range on inverter (degrees).

11.1.31 Protection

- DC fault protection (on rectifier)
  - Detection delay: Detection delay of DC fault (seconds);
  - Vd threshold: DC voltage threshold used for DC fault detection (pu);
  - α delay: Value of the constant α angle imposed after a fault is detected (degrees);
  - α delay duration: Time interval during which the value of the forced α angle is imposed by the DC protection system. (seconds);
  - α delay number: Number of times the constant α angle is imposed and then removed before the converter is automatically blocked by the DC fault protection;
- Protection against commutation failure (inverter)
  - ON/OFF Protection (1/0): “1” enables protection, “0” disables protection;
  - γ_{cf}: Value added to the lower limit of γ by the protection for commutation failures (degrees);
  - Rise time: First order time constant affecting the increase of minimum γ (seconds);
  - Fall time: First order time constant affecting the decrease of minimum γ (seconds);

11.1.32 Low AC voltage detection

- Vac threshold: Voltage threshold used for low AC voltage detection (pu)
- Detection delay: Detection delay for low AC voltage (seconds);
- Fall delay: Minimal duration of flag for low AC voltage condition (Voltage lower than Vca threshold) before the protection system start acting (seconds).

11.1.33 Disturbances

- Faults or Commutation failure (None =0, Valve= 1, DC=2, Misfiring = 3, DCY=4, DCD=5): Specifies the type of fault.
  - “0” if no disturbance is desired;
  - “1” for valve fault (short circuit);
  - “2” for ground fault on converter terminals;
  - “3” for simulation of commutation failure;

  - "4" for a fault to be applied in the converter connected to the wye secondary of the transformer
  - "5" for a fault to be applied in the converter connected to the delta secondary of the transformer
- Valve No. for fault or commutation failure (1-12): Number of valve to which the fault or the commutation failure is applied. Numbers 1 to 12 correspond to the following valves (see Figure 11 - 5): 1Y, 2Y, 3Y, 4Y, 5Y, 6Y, 1D, 2D, 3D, 4D, 5D, 6D.
- DC fault R: Value of fault resistance on converter terminals (ohm) (see Figure 11 - 5).
- Reference step (None = 0, Iref =1, Vref=2): Specifies the reference step:
  - "0" if no step is desired;
  - "1" for a step in the current reference;
  - "2"for a step in the voltage reference (see Figure 11 - 9).
- Δ Iref or Δ Vref: Step size for current or voltage reference (pu);
- Start time: Start time of the disturbance (second);
- End time: End time of the disturbance (second).

11.1.34 Valve parameters

- General parameters
  - Connection (series = Serial; delta = Delta);
- Switch parameters
  - Switch type (Breaker, Ideal Switch, Thyristor,Diode, GTO+Diode): Specifies the valve type that makes the converter;
  - Signal reset (Enable, Disable): Reset the default signal to zero.
  - Precision valve (Activé=Enable,Désactivé=Disable)
- Specific parameters
  - Rbov (Reverse break overvoltage): Highest value of reverse voltage across a valve. Relevant only for diodes, thyristors and GTOs (volts);
  - Fbov (Forward break overvoltage): Highest value of reverse voltage across a blocked valve. Relevant only for diodes, thyristors and GTOs (volts);
  - C_snubber: Snubber capacitance (farads);
  - R_snubber: Snubber resistance (ohms);
  - Tq: Turn-off time (seconds);
  - Ibreak: GTO maximum breakable current (amperes);
  - Th Roff: Open state resistance (ohms);
  - Th Ron: Closed state resistance (ohms);
  - Vf^1: Forward voltage drop (volts);
  - Ihold: Holding current.

11.1.35 Control panel for HVDC converters

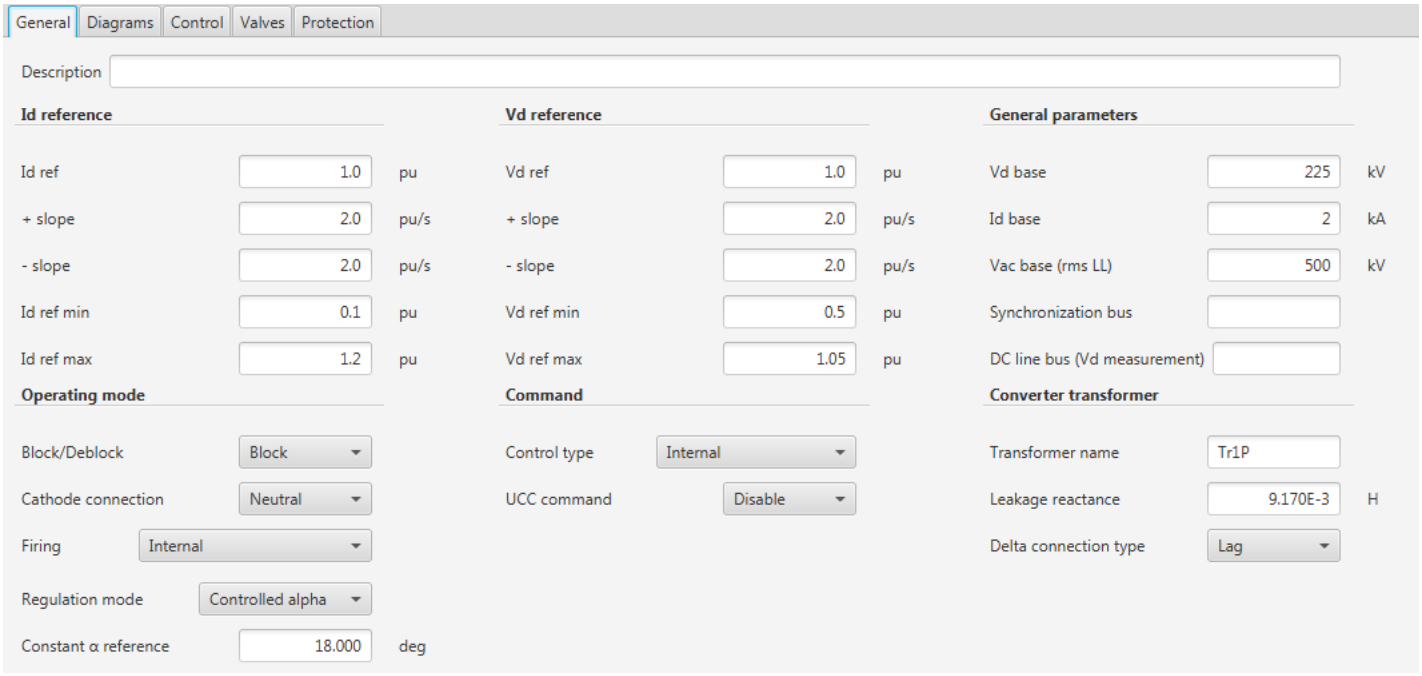


Figure 11 - 14 The parameter form for HVDC converters (General)

1.This parameter is used in the element switching logic. The forward voltage drop is not modeled.

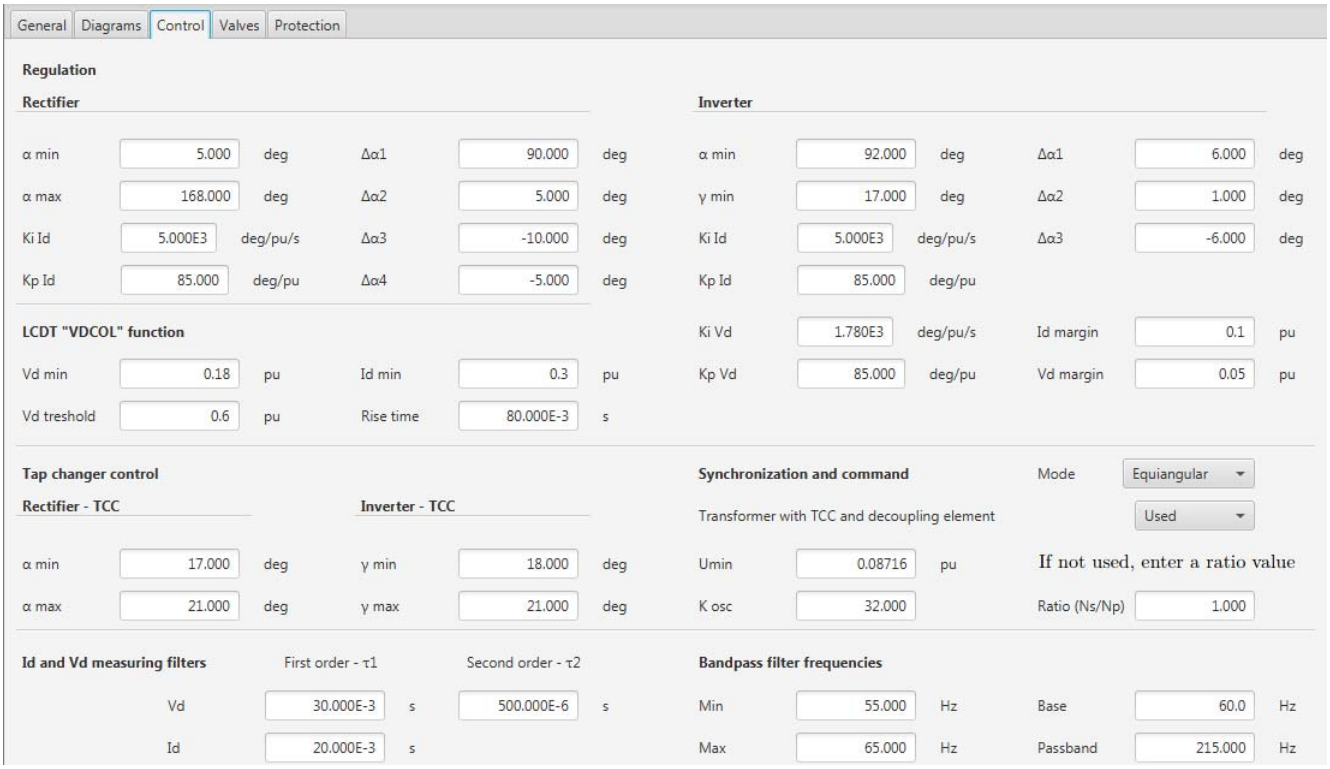


Figure 11 - 15 The parameter form for HVDC converters (Regulation)

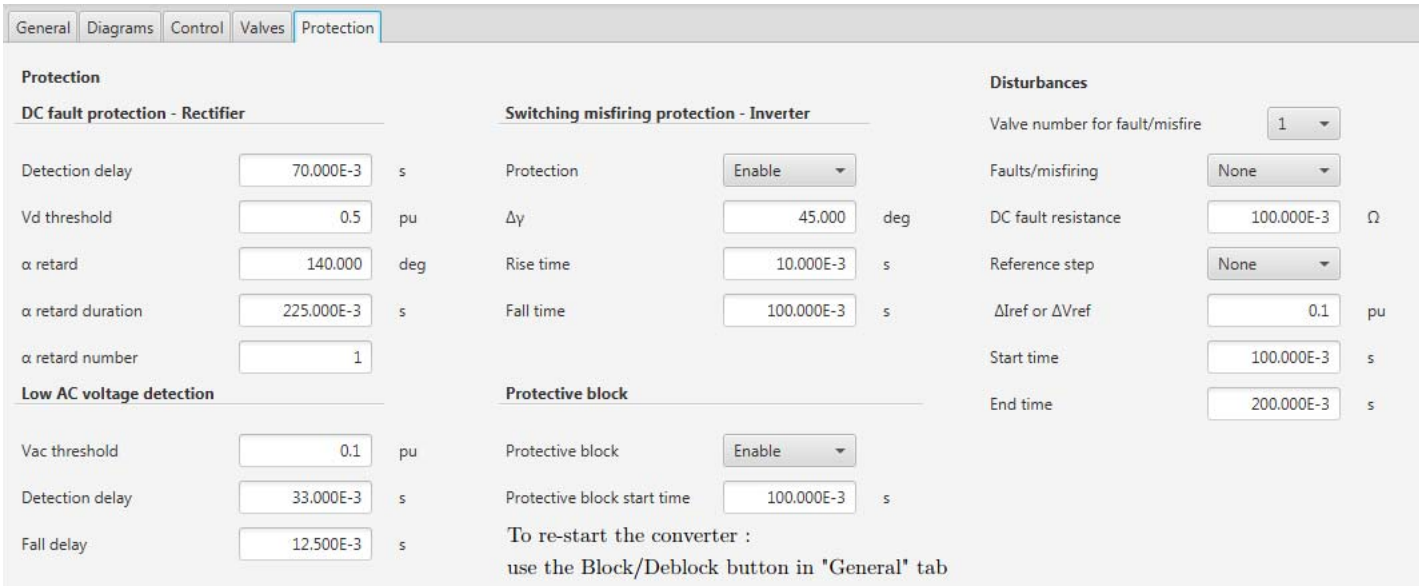


Figure 11 - 16 The parameter form for HVDC converters (Protection)

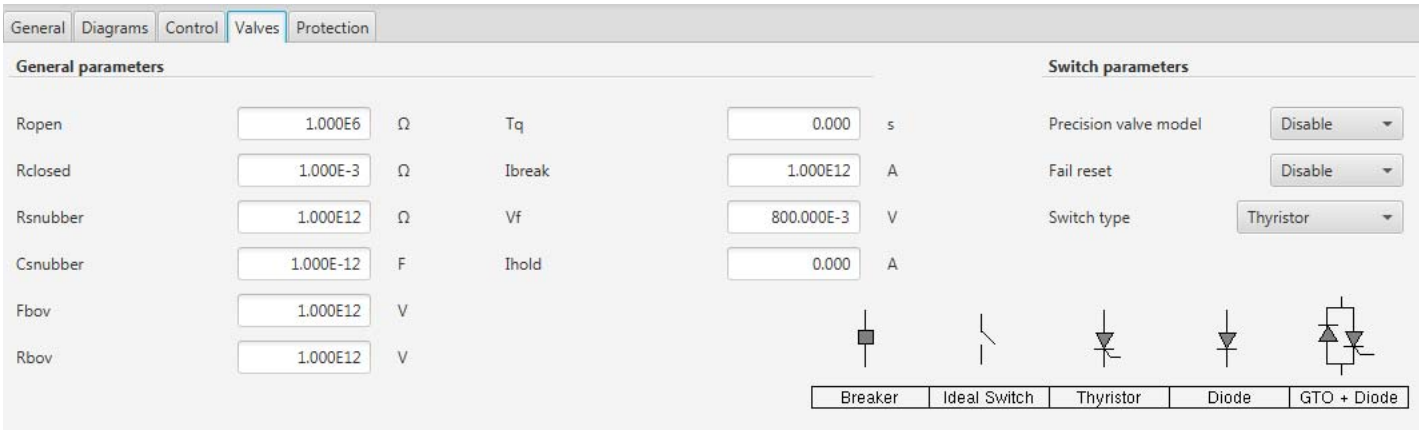


Figure 11 - 17 The parameter form for HVDC converters (Valves)

11.1.36 List of available signals

At acquisition, the following signals are made available by the **sensors**:

- VSYNCa,b,c_label: Primary phase voltages used by the firing synchronization system (volt));
- VSYNCba,cb,ac_label: Primary phase-to-phase voltages used by the firing synchronization system (volt);
- V_LINE_label: DC voltage relative to ground at the DC line input (volt);
- V_NEUTRAL_label: DC neutral relative to ground at the DC line input (volt);
- IaPrimXfo, IbPrimXfo, IcPrimXfo_label: AC currents in the primary windings of the transformer (ampere);
- Id_label: DC current on bridge (ampere);
- IaY, IbY, IcY_label: AC currents in the Y secondary windings of the transformer (ampere);
- V12_xY_label (x = 1, 2, 3, 4, 5, 6): Voltage across valve x of the bridge connected to the Y windings (volt);
- I12_xY_label (x = 1, 2, 3, 4, 5, 6): Current across valve x of the bridge connected to the Y windings (Amperes);
- CMD12INT_xY_label (x = 1,2,3,4,5,6): Firing command from the internal source to component “1 to 2” of valve x of the bridge connected to the Y windings (logical);
- CMD21INT_xY_label (x=1,2,3,4,5,6): Firing command from the internal source to component “2 to 1” of valve x of the bridge connected to the Y windings (logical);
- CMD12EXT_xY_label (x=1,2,3,4,5,6): Firing command from the external source to component “1 to 2” of valve x of the bridge connected to the Y windings (logical);
- CMD21EXT_xY_label (x=1,2,3,4,5,6): Firing command from the external source to component “2 to 1” of valve x of the bridge connected to the Y windings (logical);
- CMDFLT_ label: Flag for a valve fault (logical);

- PPattern_label: A number whose binary code specifies that the thyristors are receiving firing pulses. For example, 5 specifies that firing pulses are sent to thyristors 1 and 3.
- Up_Trlabel: Signal sent to the tap changer to increase the tap position (logical);
- Down_Trlabel: Signal sent to the tap changer to decrease the tap position (logical);
- STATE12_xY_label (x = 1,2,3,4,5,6): State of the “1 to 2” component of valve x of the bridge connected to the Y windings (logical));
- STATE21_xY_label (x = 1,2,3,4,5,6): State of the “2 to 1” component of valve x of the bridge connected to the Y windings (logical);
- FAILSIG_xY_label (x = 1,2,3,4,5,6): Valve alarm signal with the following meanings:
  - 1: Infringement of Tq extinction limit time for Thyristor 12. (Automatically reset to zero after a time step).
  - 1: Infringement of Tq extinction limit time for Thyristor 21. (Automatically reset to zero after a time step).
  - 2: Reverse voltage of Thyristor 12 greater than Rbov. (Reset to zero only if Fail Reset= Enable.
  - 2: Reverse voltage of Thyristor 21 greater than Rbov. (Reset to zero only if Fail Reset= Enable.
  - 3: Direct voltage of Thyristor 12 greater than Rbov. (Reset to zero only if Fail Reset= Enable.
  - DelayImpInt_label: Internal pulse delay.
- DelayImpExt_label: External pulse delay.
- DelayImp_label: Pulse delay.
- DelayImpUsed_label: Pulse delay used.
- P_label: Same as Pattern_label, but originating from control module.
- D_label: Delay from control module.
- IaD, IbD, IcD_label: AC current in the delta secondary windings connected to transformer (ampere);
- V12_xD_label (x=1, 2, 3, 4, 5, 6): Voltage in valve x of the bridge connected to the delta windings (volt);
- I12_xD_label (x=1, 2, 3, 4, 5, 6): Current in valve x of the bridge connected to the delta windings (ampere);
- CMD12INT_xD_label (x=1,2,3,4,5,6): Firing command from the internal source to component “1 to 2” of valve x of the bridge connected to the delta windings (logical). For the GTO+Diode switch the signal value is -1 when the diode is forced to conduct;
- CMD21INT_xD_label (x=1,2,3,4,5,6): Firing command from the internal source to component “2 to 1” of valve x of the bridge connected to the delta windings (logical);
- CMD12EXT_xD_label (x=1,2,3,4,5,6): Firing command from the external source to component “1 to 2” of valve x of the bridge connected to the delta windings (logical);

- CMD21EXT_xD_label (x=1,2,3,4,5,6): Firing command from the external source to component “2 to 1” of valve x of the bridge connected to the delta windings (logical). For the GTO+Diode switch the signal value is -1 when the diode is forced to conduct;
- STATE12_xD_label (x = 1,2,3,4,5,6): State of the “1 to 2” component of valve x of the bridge connected to the delta windings (logical);
- STATE21_xD_label (x = 1,2,3,4,5,6): State of the “2 to 1” component of valve x of the bridge connected to the delta windings (logical);
- FAILSIG_xD_label (x = 1,2,3,4,5,6):
- PeriodY_label: Period of AC voltage measured in the "equiangular" synchronization system of the bridge connected to the Y windings (seconds);
- PeriodD_label: Period of AC voltage measured in the "equiangular" synchronization system of the bridge connected to the delta windings (seconds);
- IdRef_label: DC current reference (pu);
- VdRref_label: DC voltage reference (pu);
- Mu_label: Commutation angle (degrees);
- Gamma_label: Extinction angle (degrees);
- Alpha_label: Firing delay angle generated by the regulation system (degrees);
- Deblocked_label: Unblocking status flag (logical);
- CmdComFail_label: Command to simulate a switching failure (logical);
- CmdInvMode_label: Specifies the rectifier/inverter mode (0 = rectifier; 1 = inverter) (logical);
- ComFail_label: Detection signal for a switching failure on Y or delta bridge (logical);
- AlphaRet_label: Signal specifying the forced retard mode (logical).
- RatioXfo_label: Normalized transformation ratio (Ns/Np) of converter transformer (pu);
- syn_Vd0_level_label: Mean of the maximum ideal DC voltage (pu) - in the equidistant synchronization system;
- syn_Alpha_Osc_label: Firing delay angle reflecting the oscillator phase (degrees) - in the equidistant synchronization system;
- syn_Alpha_measured_label: Measured firing delay angle (degrees) - in the equidistant synchronization system;
- syn_Delta_alpha_label: Phase variation (positive = lag; negative = lead) of oscillator (degrees) - in the equidistant synchronization system;
- syn_Vac_ZC_number_label: Count for the 12 zero crossings of switching voltages in the 12 pulse converter [0 to 11] - in the equidistant synchronization system. The 0 count coincides with the zero crossing of the switching voltage of valve 1 on the Y bridge (D) when the delta winding is lagging (or ahead) of the Y winding;

- syn_Firing_pulse_number_label: Count for the 12 firing of the valves in the 12 pulse converter [0 to 11] - in the equidistant synchronization system. The 0 count coincides with the firing pulse of valve 1 on the Y bridge (D) when the delta winding is lagging (or ahead) of the Y winding;
- sys_Frequency_label: Measured frequency of AC voltage (Hz) - in the equidistant type synchronization system.

11.2 SVC CONTROLLER

A – Introduction

This model represents the power component and the control system of a static compensator. The power component consists of a thyristor controlled reactor (TCR inductive branch) and three thyristor switched capacitors (TSC capacitive branches). The transformer is not modeled internally and must be added by the user.

The control system includes measuring, synchronization, regulation, distribution and firing subsystems. Depending on the operation mode, the model allows users to study step responses either for a voltage reference or a susceptance reference. This feature can be used to optimize the regulator parameters.The thyristors can also be fired by signals generated from an external source.

B – Static Compensator Icon and Diagram

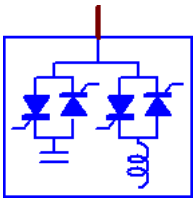


Figure 11 - 18 Static compensator icon and diagram.

C – Static Compensator Model

Figure 11 - 19 shows the static compensator diagram.

2 Power Component – The models of the four branches of a static compensator are identical (see Figure 11 - 20). Resistances R and r respectively represent ohmic losses in the capacitor and the reactor. One of these elements can be ignored by assigning a zero value to it in the control panel. The two resistances, the capacitor and the reactor form a type of black box. Hence, it is not possible to measure the voltage across one of the resistances or the reactor. However, the voltage across the capacitor is calculated and available as a signal. This is also the case for the voltages across the thyristors.

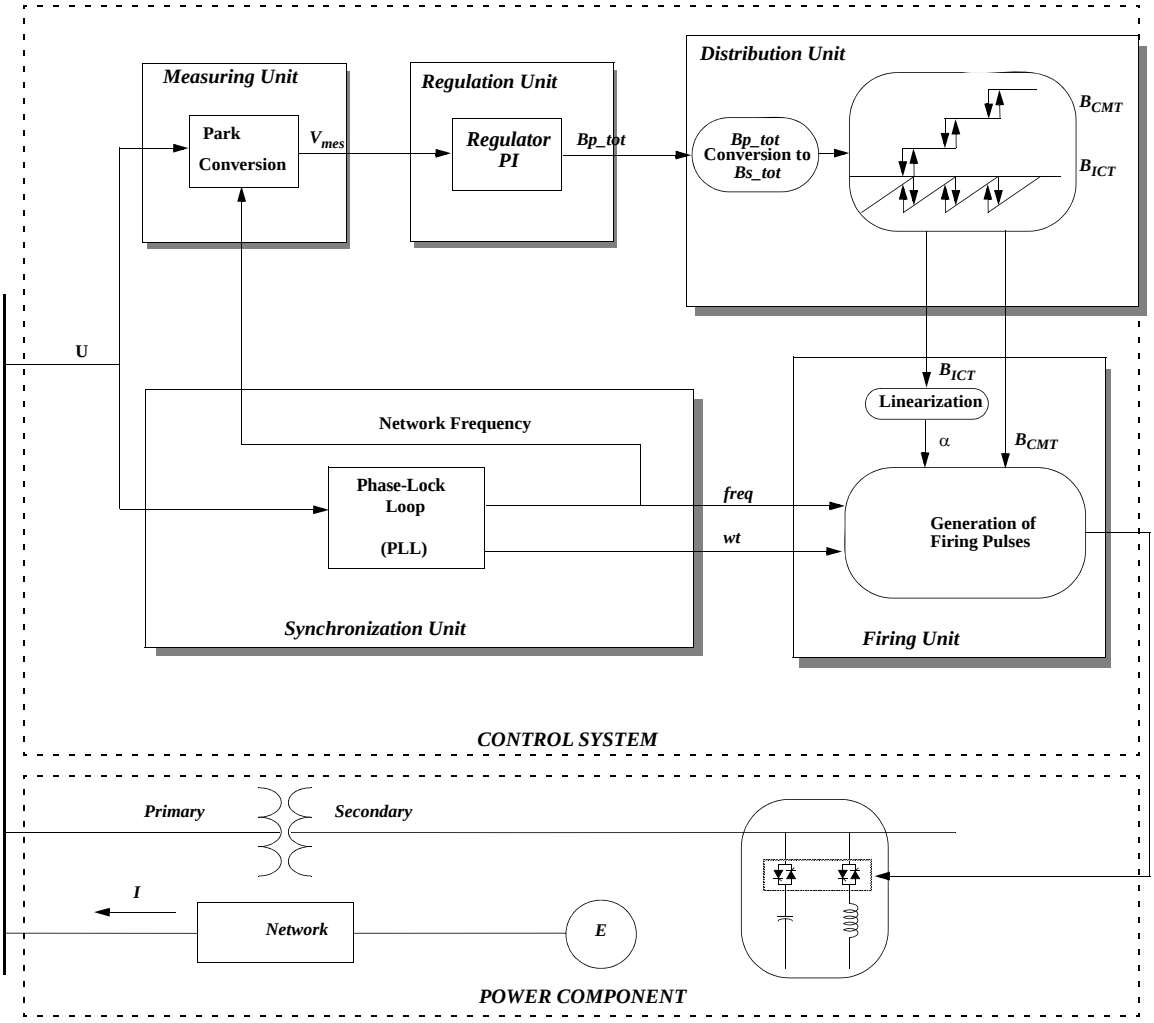


Figure 11 - 19 Static compensator diagram

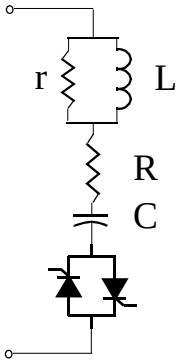


Figure 11 - 20 Static compensator branch

D – Control System

- Synchronization Unit

  The synchronization unit consists of a phase-lock loop (PLL) applied to each voltage phase on the transformer primary. The PLL calculates the frequency and phase angle required to fire the thyristors. Figure 11 - 21 shows a simplified diagram of this unit. This type of synchronization has the advantage of being insensitive to harmonics and stable in frequency.

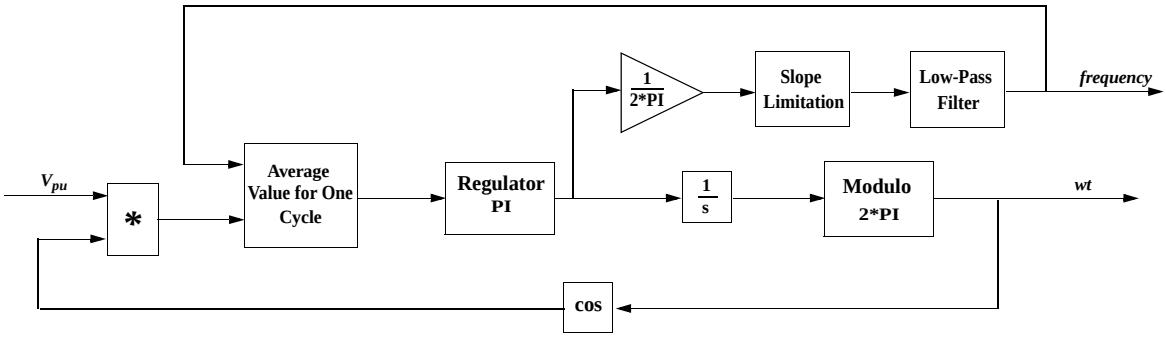


Figure 11 - 21 Phase-Lock Loop (PLL)

- Measuring Unit

  Voltage measuring must be accurate, fast and insensitive to harmonics. To do this, the output of the Park conversion block is integrated and the voltage is measured by subtracting two consecutive samples of the integrator output with a delay of one cycle between them. The voltage measuring unit is shown in Figure 11 - 22.

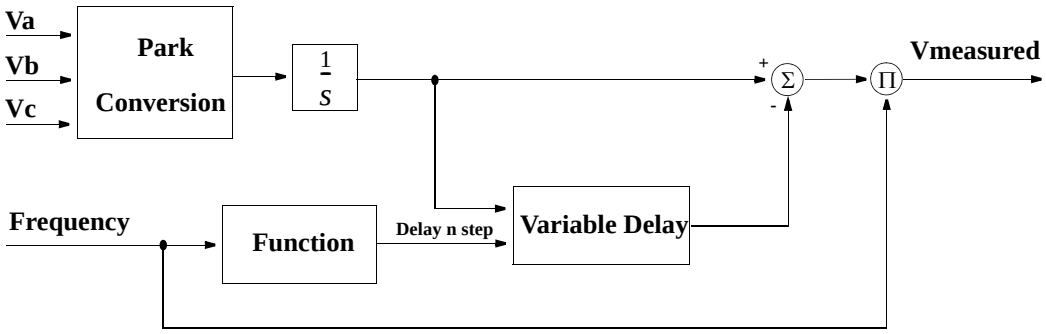


Figure 11 - 22 Measuring Unit

- Control Unit

  The control unit consists of a proportional and integral (PI) controller. The latter compares the voltage measured and voltage reference to achieve:

$$U_{mes} = U_{ref} + X_{sI} \quad \text{(EQ 11)}$$

  The output of the controller is given by:

$$B_p = \left(K_p + \frac{K_i}{s}\right) \times (U_{mes} - U_{ref} - X_{sI}) \quad \text{(EQ 12)}$$

  Bp is the required susceptance on the primary side for regulation. The current I is not measured but calculated using *Bp* and *Umes*. The response of the controller depends on the value of the gains. The integral gain determines the speed of the controller, while the proportional gain can be used to compensate for the delay in the firing system.

- Distribution Unit

  The distribution unit receives the following input:

  – The leakage inductance of the transformer;
  – The signal *Bp* from the *PI;*
  – The states and values of each TSC capacitive and TCR inductive branch;
  – And the value of the hysteresis to apply at transition points.

  From the primary susceptance *Bp* of the static compensator and the leakage inductance of the transformer, the susceptance *Bs* on the secondary side is calculated and then represented as a parallel combination of the TSC capacitive and TCR inductive branches.

$$B_s = B_{ind} + B_{cap} \quad \text{(EQ 13)}$$

  The value of the capacitance *Bcap* produced by the parallel capacitive branches and the value of *Bind* is given by the non-linear function:

$$B_{ind} = \frac{2\pi - 2\alpha + \sin 2\alpha}{\pi} \quad \text{(EQ 14)}$$

The calculation of the equivalent impedance of the parallel TSC capacitive branches take into account the availability of the branches. Therefore, it is possible to operate in downgraded or degradation mode.

In order to avoid oscillations when the capacitors are switched, hysteresis is used at transition points when the number of parallel TSC capacitive branches changes.

- Firing Unit

  The function of the firing unit is to send the firing orders to the thyristors of the different branches. To do this, it receives the following input:

  – Phase angle (ωt) of the synchronization voltage;
  – Firing angle α;
  – Firing order of the TSC capacitive branches.

  Since the TCR inductive branch is controlled, the firing unit sends the αt degree pulses after the last zero-crossing of the synchronization voltage. Since the TSC capacitive branches are only switched and not controlled, their firing is always executed at the same time on the waveform, that is 90 degrees before the zero-crossing of the voltage.

11.2.1 Parameters

A – General Parameters

- Transformer Parameters
  – Name of primary XFO Bus: Name of the bus on the high voltage side of the static compensator transformer;
  – Primary XFO V: Line-line rated voltage on the primary side of the transformer (kV rms);
  – Secondary XFO V: Line-line rated voltage on the secondary side of the transformer (kV rms).
  – Leakage: Leakage inductance of the primary winding of the transformer (pu/100MVA);
  – Δ vs Y (Lag, Lead): Specifies the connection of the transformer and the Delta windings lagging or preceding the Y winding.
- Control System Parameters
  – Source of control: Where the control system is modelized (Intern = Internal, External, Simulink);
  – Firing order: (Internal, External);
  – Directory: Directory where the HyperLink model is saved;
  – Name of HyperLink model;
  – Execution time: Estimated execution time for the HyperLink model.
  – Precision valve: Specifies if the user wants to use the precision valve model

11.2.2 Control System Parameters

A – Reference Parameters

- Vref: Voltage reference (pu) (automatic mode);
- Bref: Susceptance reference (pu/100MVA) (manual mode).
- CLC Mode: (Automatic, Manual)

B – Operating Mode Parameters

- TCC mode: (On = synchronized firing of the TSC capacitive branches, Off = continuous firing);
- Valve blocking and unblocking: (Deblock = valve firing enabled, Block = valve firing disabled);

C – Regulation Parameters

- Kp: Proportional gain;
- Ki: Integral gain;
- Pente: Slope of voltage controller (pu/100MVA);
- Hysteresis: (pu/100MVA).

D – Protection Strategies

- Vmax: Maximum value of primary voltage (pu). Above this value, the static compensator is disabled;
- Vmin_on: Minimum value of primary voltage (pu). Below this value, the static compensator is disabled;
- Vmin_off: Minimum value of primary voltage (pu) required to enable the static compensator.

E – AC Fault Parameters

- Vac_min: Primary voltage threshold (pu) below which a fault is detected;
- Delay AC fault (s);
- Minimum duration - AC fault (s);
- Delay under voltage: falling edge delay during a specified time interval is applied (s).

F – Disturbance Parameters

- Disturbance type: Vref or Bref;
- Delta_Vref: Value of step in the voltage reference (pu);
- Delta_Bref: Value of step in the value of the susceptance reference (pu/100MVA);
- Start time: Time when the disturbance is applied (s);
- End time: Time when the disturbance is removed (s).

G – Adaptive Band-Pass Parameters

- Base frequency (Hz);
- Minimum frequency (Hz);
- Maximum frequency (Hz);
- Bandwidth (Hz).

H –Power Component Parameters

The parameters of the elements in the compensator power component are the same for all four branches.

- General Parameters
  - Connections: Y ground; Y floating; Delta.
- RLC Element Parameters
  - Branch reactor (H);
  - Resistance in parallel with branch reactor (Ω) ;
  - Branch resistance (Ω);
  - Branch capacitor (F).
- Back-to-back Valve Parameters
  - Valve resistance when open (Ω);
  - Valve resistance when closed (Ω);
  - Threshold voltage (V);
  - Chopping current (A);
  - Snubber resistance (Ω);
  - Snubber capacitor (F);
  - Reverse break overvoltage (V);
  - Forward break overvoltage (V).

11.2.3 List of Available Signals

At acquisition, the following signals are made available by the **sensors**:

- CMD12*phase*_TCR1_*label*: Firing pulse of the positive valve in the TCR inductive branch;
- CMD21*phase*_TCR1_*label*: Firing pulse of the negative valve in the TCR inductive branch;
- I*phase*_TCR1_*label*: Current across the TCR inductive branch;
- STATE12*phase*_TCR1_*label*: State of the positive valve in the TCR inductive branch;
- STATE21*phase*_TCR1_*label*: State of the negative valve in the TCR inductive branch;
- V*phase*Th_TCR1_*label*: Voltage across the valves in the TCR inductive branch;
- VCAP*phase*_TCR1_*label:* Voltage across the capacitor in the TCR inductive branch;

- FAILSIG*phase*_TCR1_*label:*;
- CMD12*phase*_TSC1_*label*: Firing pulse of the positive valve in TSC capacitive branch no 1;
- CMD21*phase*_TSC1_*label*: Firing pulse of the negative valve in TSC capacitive branch no 1;
- I*phase*_TSC1_*label*: Current across TSC capacitive branch no 1;
- STATE12*phase*_TSC1_*label*: State of the positive valve in TSC capacitive branch no 1;
- STATE21*phase*_TSC1_*label*: State of the negative valve in TSC capacitive branch no 1;
- V*phase*Th_TSC1_*label*: Voltage across the valves in TSC capacitive branch no 1;
- VCAP*phase*_TSC1_*label*: Voltage across the capacitor in TSC capacitive branch no 1;
- FAILSIG*phase*_TSC1_*label*:
- CMD12*phase*_TSC2_*label*: Firing pulse of the positive valve in TSC capacitive branch no 2;
- CMD21*phase*_TSC2_*label*: Firing pulse of the negative valve in TSC capacitive branch no 2;
- I*phase*_TSC2_*label*: Current across TSC capacitive branch no 2;
- STATE12*phase*_TSC2_*label*: State of positive valve in TSC capacitive branch no 2;
- STATE21*phase*_TSC2_*label*: State of negative valve in TSC capacitive branch no 2;
- V*phase*Th_TSC2_*label*: Voltage across the valves in TSC capacitive branch no 2;
- VCAP*phase*_TSC2_*label*: Voltage across the capacitor in TSC capacitive branch no 2;
- FAILSIG*phase*_TSC3_*label:*
- CMD12*phase*_TSC3_*label*: Firing pulse of the positive valve in TSC capacitive branch no 3;
- CMD21*phase*_TSC3_*label*: Firing pulse of the negative valve in TSC capacitive branch no 3;
- I*phase*_TSC3_*label*: Current across TSC capacitive branch no 3;
- STATE12*phase*_TSC3_*label*: State of positive valve in TSC capacitive branch no 3;
- STATE21*phase*_TSC3_*label*: State of negative valve in TSC capacitive branch no 3;
- V*phase*Th_TSC3_*label*: Voltage across the valves in TSC capacitive branch no 3;
- VCAP*phase*_TSC3_*label*: Voltage across the capacitor in TSC capacitive branch no 3;
- FAILSIG*phase*_TSC3_*label:*
- pulsePat_int_*label*: Signal containing the binary code representing the firing orders of the valves
- VSYNC*phase_label*: Voltage signal used by synchronization unit;
- DelayImpInt_ *label*: Firing delay (as a fraction of calculation step) calculated by the internal command of the static compensator

- DelayImpExt_ *label:* Firing delay (as a fraction of calculation step) calculated by an external command of the static compensator
- DelayImp_ *label:* Firing delay (as a fraction of calculation step) sent to the static compensator
- DelayImpUsed_ *label:* Firing delay (as a fraction of calculation step) used by the static compensator
- V_Ref_*label*: Voltage reference for the controller;
- B_Ref_*label*: Susceptance reference for the controller;
- Slope_*label*: Slope of the controller;
- Deblocked_*label*: Signal specifying that the firing pulses are blocked or not.
- TCC_Mode_*label*: Signal specifying that the TCC mode is enabled or disabled
- ManualMode_*label*: Signal specifying that the manual mode is enabled or disabled
- Period_*label*: Period of the network (inverse of the frequency)
- Frequency_*label*: Network frequency
- Alpha_TCR1_*label*: Firing angle of the TCR inductive branch
- wt*phase_label*: Phase angle of synchronization voltages
- V_Prim_*label*: Voltage measured by the system
- V_Error_*label*: Input of PI regulator of regulation unit
- B_SVC_*label*: Susceptance seen from primary side of transformer
- B_TSC_*label*: Capacitive susceptance required
- B_TCR_*label*: Inductive susceptance required

A – Static Compensator Control Panel

Figures 11 - 23 to 11 - 25 show respectively the first, second and third pages of the static compensator control panel.

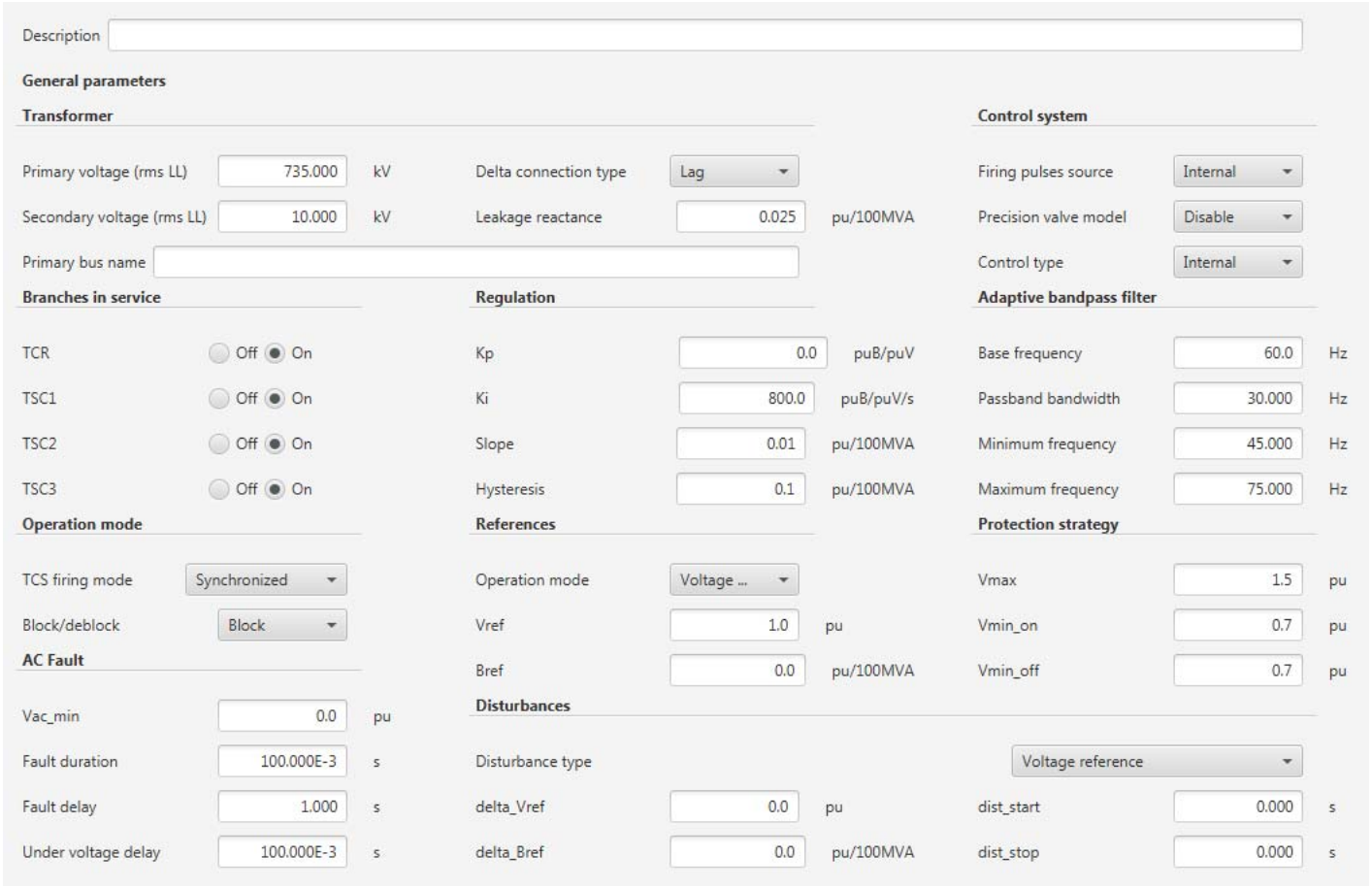


Figure 11 - 23 Static compensator control panel (General)

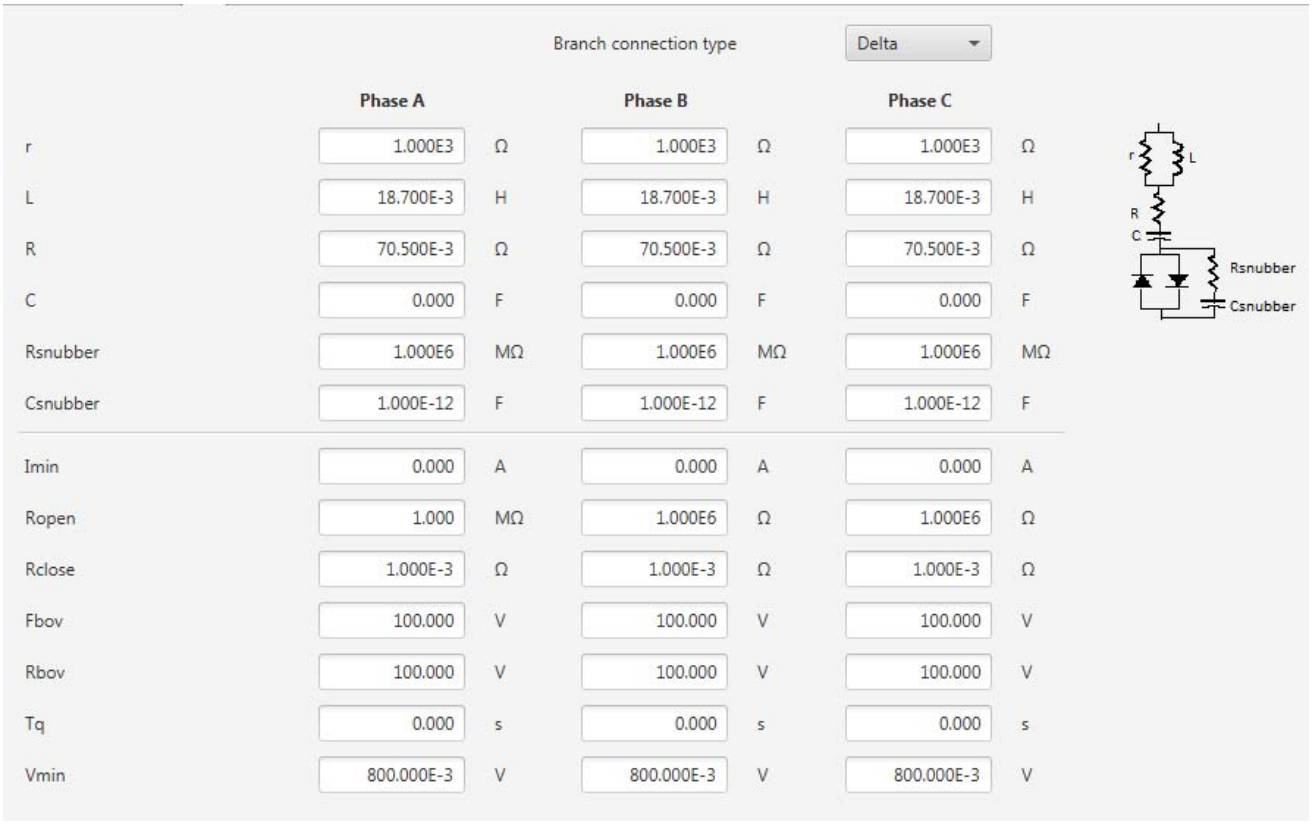


Figure 11 - 24 Static compensator control panel (TCR)

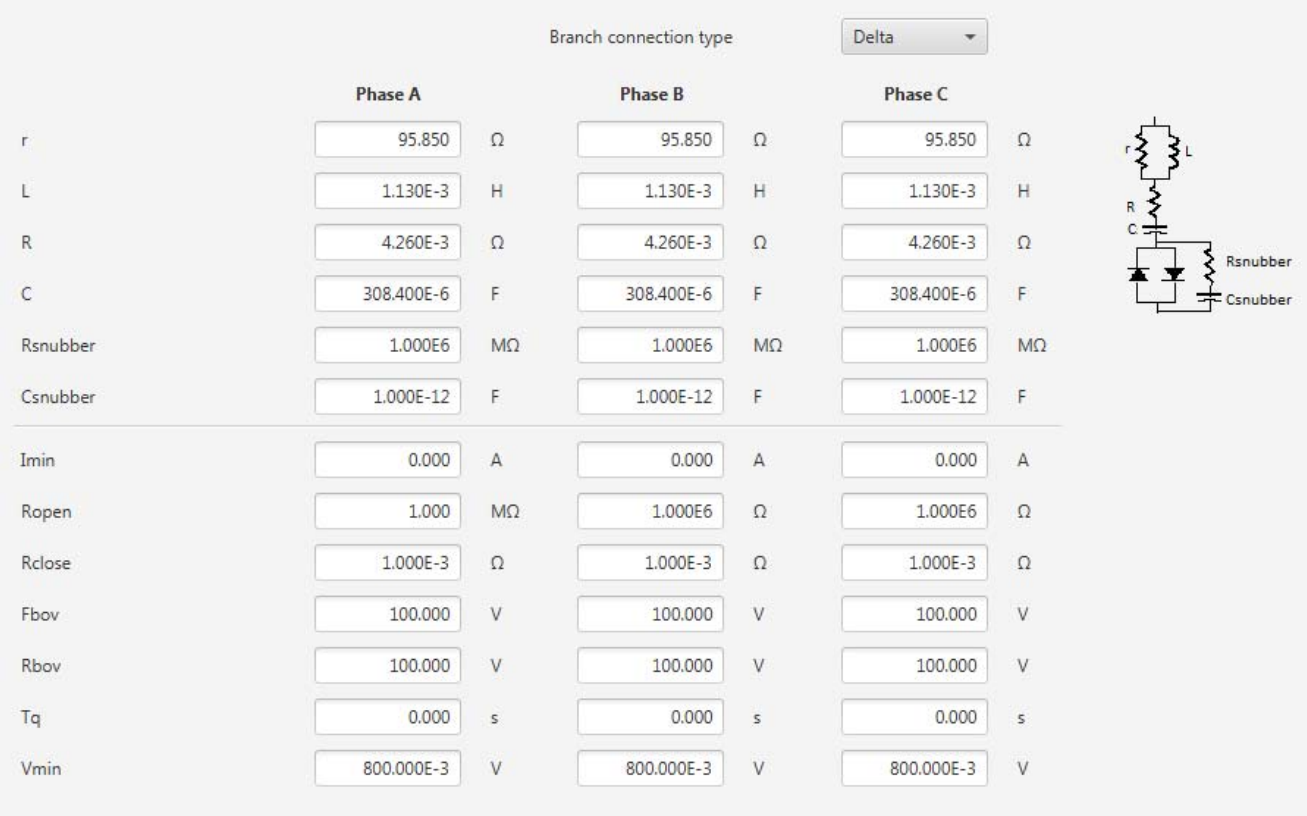


Figure 11 - 25 Static compensator control panel (TSC1)

Figure 11 - 26 shows the network used in this example. The test consists in applying a rising ramp from 0.75 to 1.25 pu to the source voltage. Then a positive sequence reading is taken of the voltage on the transformer primary and of the current in the Rprim resistance to draw the U-I dynamic curve of the system. The variation of the source voltage is done as a ramp over 10 seconds.

The following parameters are used:

- Static Compensator: Fault parameters, automatic mode at Vref = 1.0 pu
- Network at 735 kV, short-circuit power of 6000 MVA, quality factor of 10
- Transformer YD 735/16 kV, 333 MVA, leakage of 15%
- Load on primary = 200 MW
- Load on secondary = 500 kW

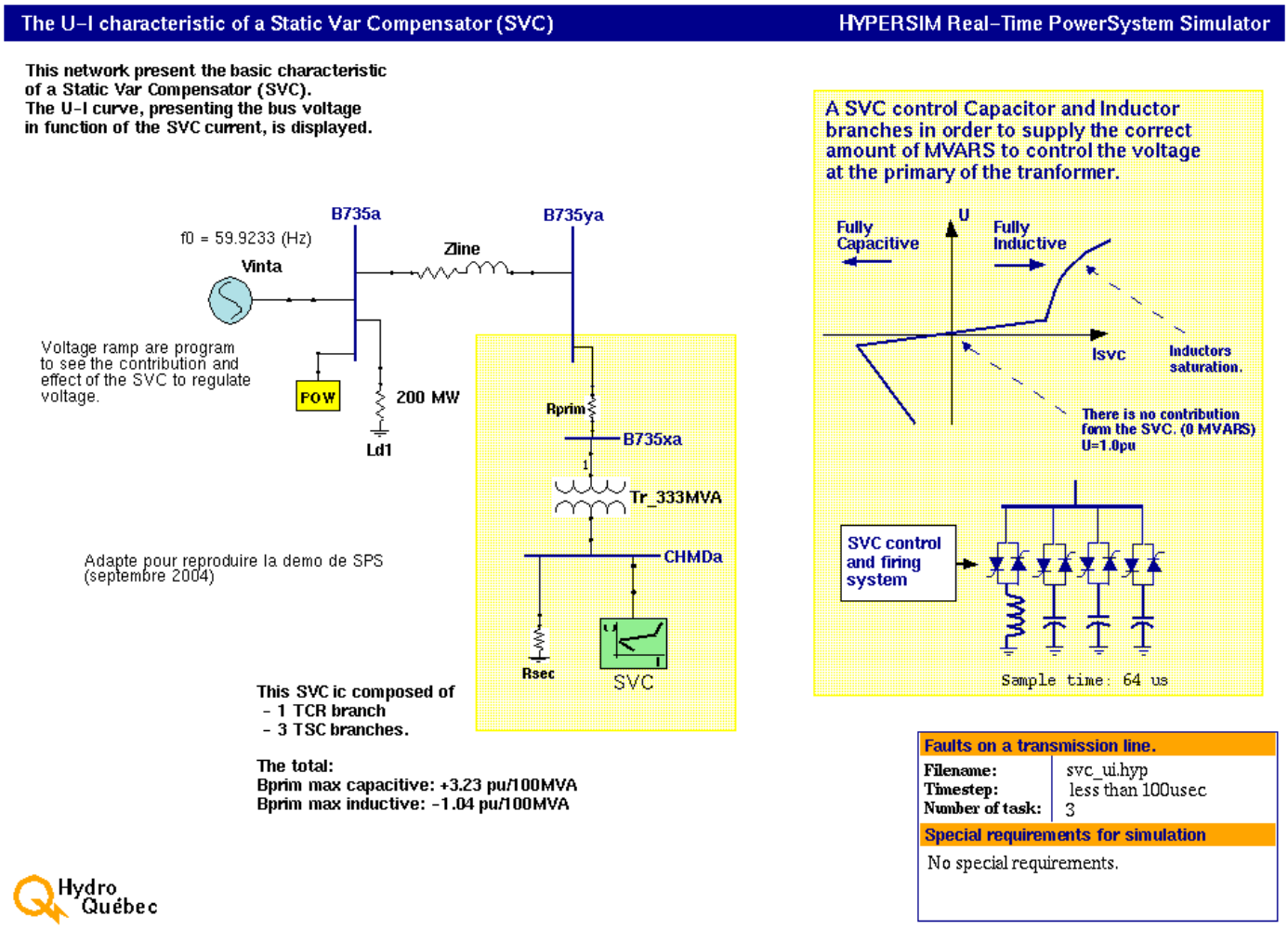


Figure 11 - 26 Test network for the static compensator

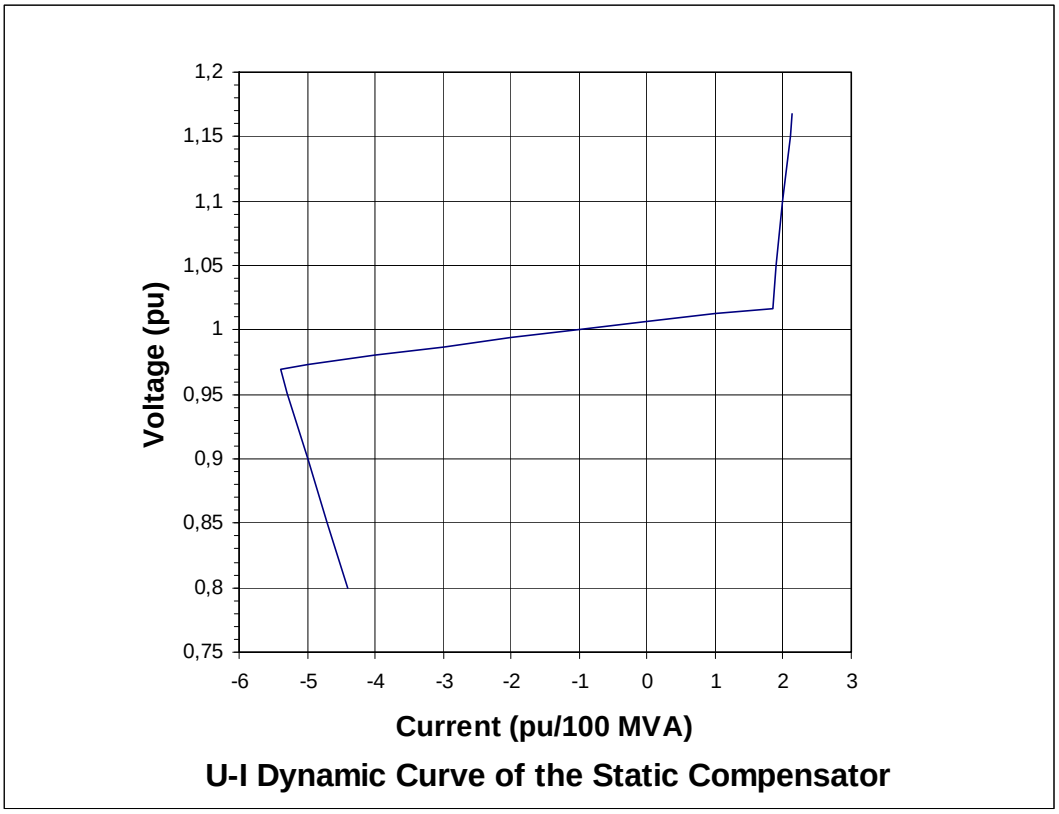


Figure 11 - 27 U-I dynamic curve of the static compensator

11.3 STATIC COMPENSATOR BRANCHES: TCR AND TSC

As seen in the introduction to this chapter, the static compensator model consists of a control system and a power component. The latter has 4 three-phase branches, each with the same configuration, as shown in Figure 11 - 20. The model presents a configuration with one TCR inductive branch and three TSC capacitive branches. However, the user may want to build their own static compensator model with a different configuration. They can then use the static compensator branch model with an external control. which they can program themselves. Both types of branches are available to the user: the TCR inductive branch (TCR or thyristor-controlled reactor) and the TSC capacitive branch (TSC or thyristor-switched capacitor). Essentially, both of these models are identical, the TCR branch being a specific case of the TSC branch.

These models are built-in and do not add nodes (or increase the Z matrix).

A – Icons and Diagrams of TCR and TSC Static Compensators

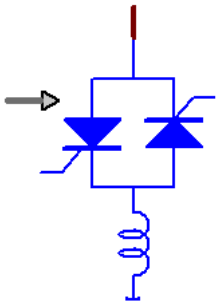


Figure 11 - 28 TCR inductive branch icon and diagram

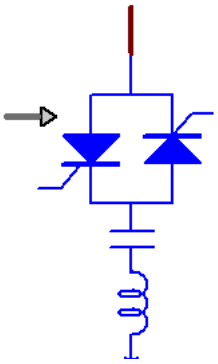


Figure 11 - 29 TSC capacitive branch icon and diagram

B – Parameters

The parameters for both types of static compensator are identical to those shown in section 11.2.1.

C – List of Available SIgnals

- CMD12*phase_label*: Firing pulse in the positive valve;
- CMD21*phase_label*: Firing pulse in the negative valve;
- I*phase_label*: Current across the branch;
- STATE12*phase_label*: State of the positive valve;
- STATE21*phase_label*: State of the negative valve;
- VCAP*phase_label*: Voltage across the capacitor (volt);
- DelayImpInt_ *label*: Firing delay (as a fraction of calculation step) calculated by the internal command (not used)
- DelayImpExt_ *label:* Firing delay (as a fraction of calculation step) calculated by an external command
- DelayImp_ *label:* Firing delay (as a fraction of calculation step) sent to the valves
- DelayImpUsed_ *label:* Firing delay (as a fraction of calculation step) used

The signals are the same for both types of branches. Of course, the voltage across the capacitor of the TCR inductive branch will always be null.

D – Control Panels of TCR and TSC Static Compensators

Figures 11 - 30 and 11 - 31 show respectively the TCR inductive branch and TSC capacitive branch control panels.

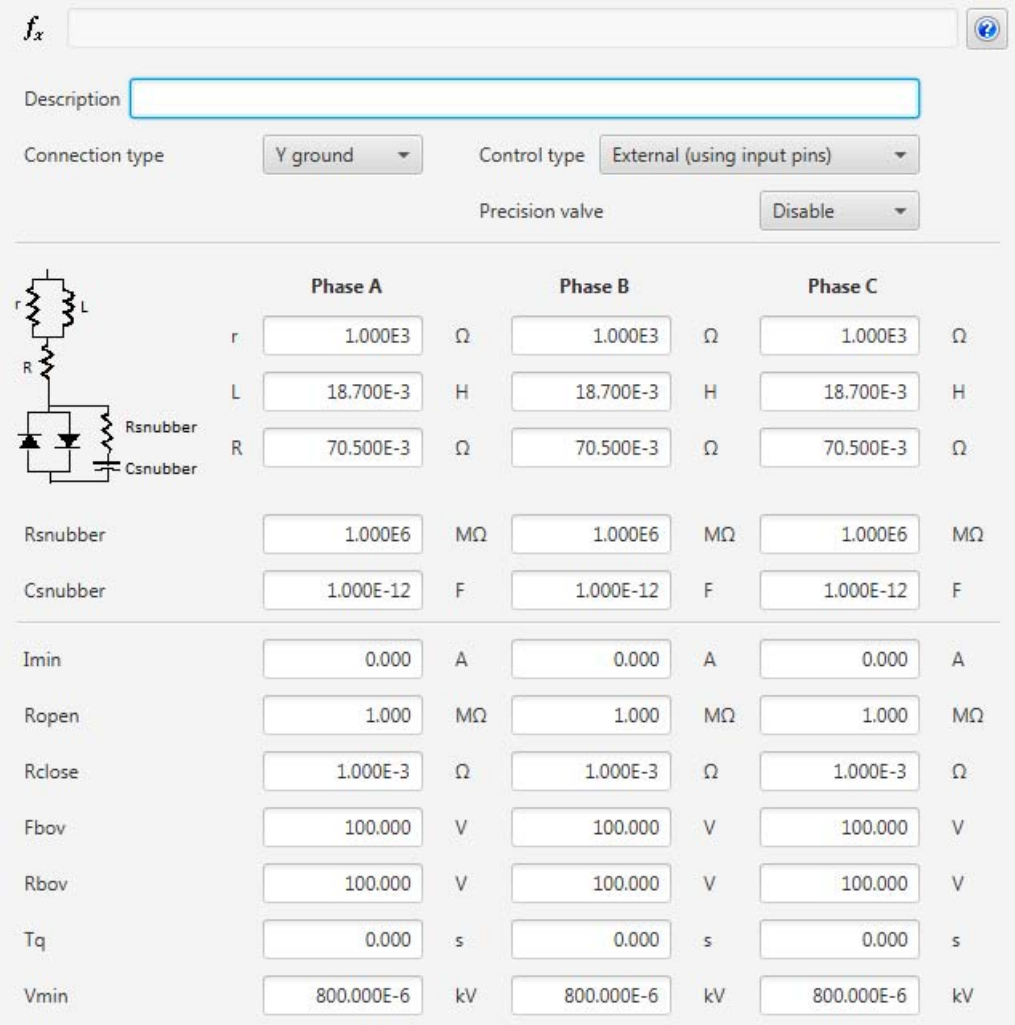


Figure 11 - 30 TCR inductive branch control panel

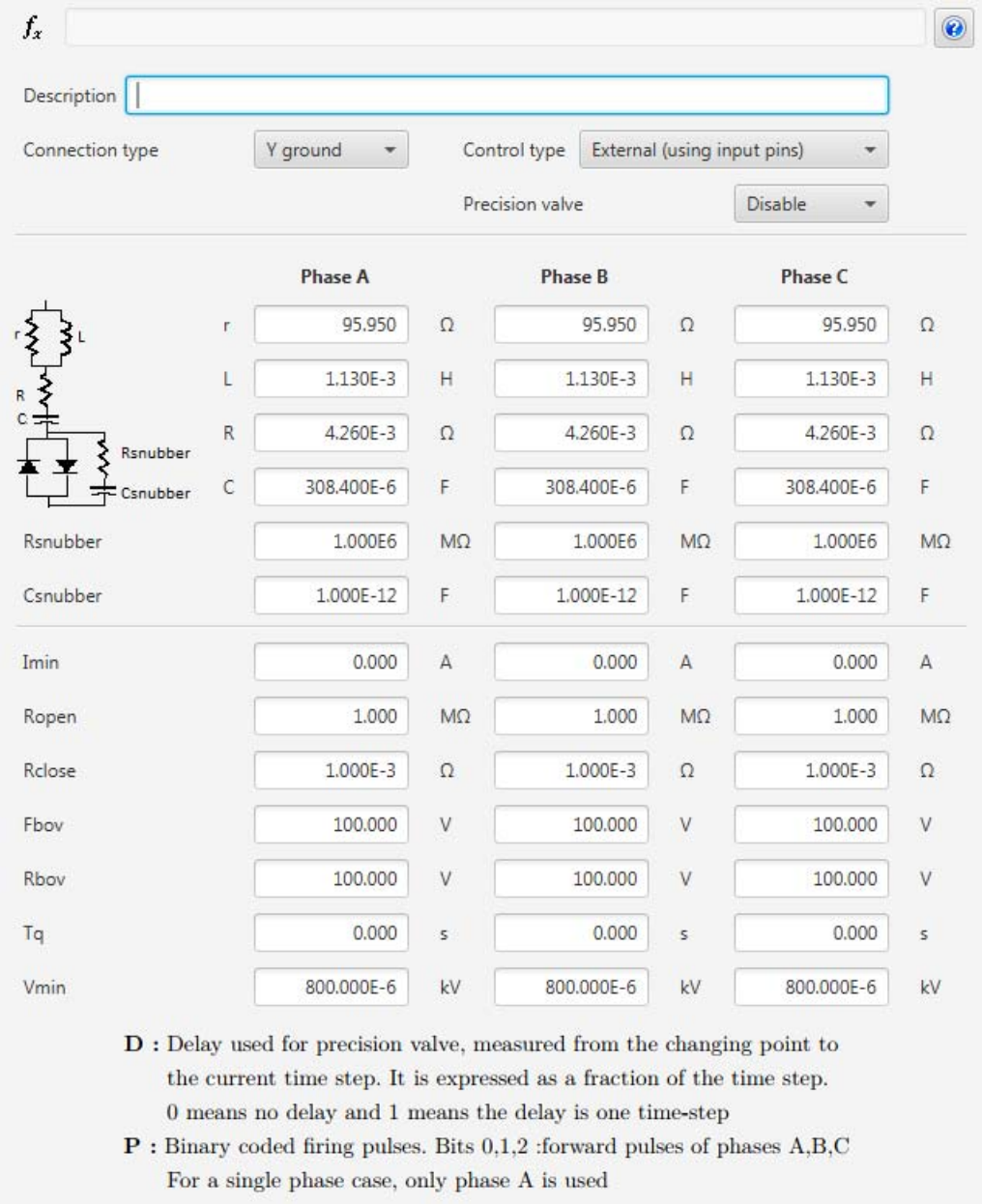


Figure 11 - 31 TSC capacitive branch control panel

This example shows the use of a static compensator branch and is very similar to the static compensator model described previously. The network in Figure 11 - 32 is identical to that in Figure 11 - 26, the only difference being in the static compensator. In this case, the power component is simulated with static compensator branches and the control system with a HyperLink block. The static compensator being simulated consists of two TSC capacitive branches and one TCR inductive branch. The powers of the branches are identical to those of the static compensator in the preceding example.

The same test is made, a voltage ramp of 0.75 to 1.25 pu over 10 seconds. The results of the test are shown in Figure 11 - 33.

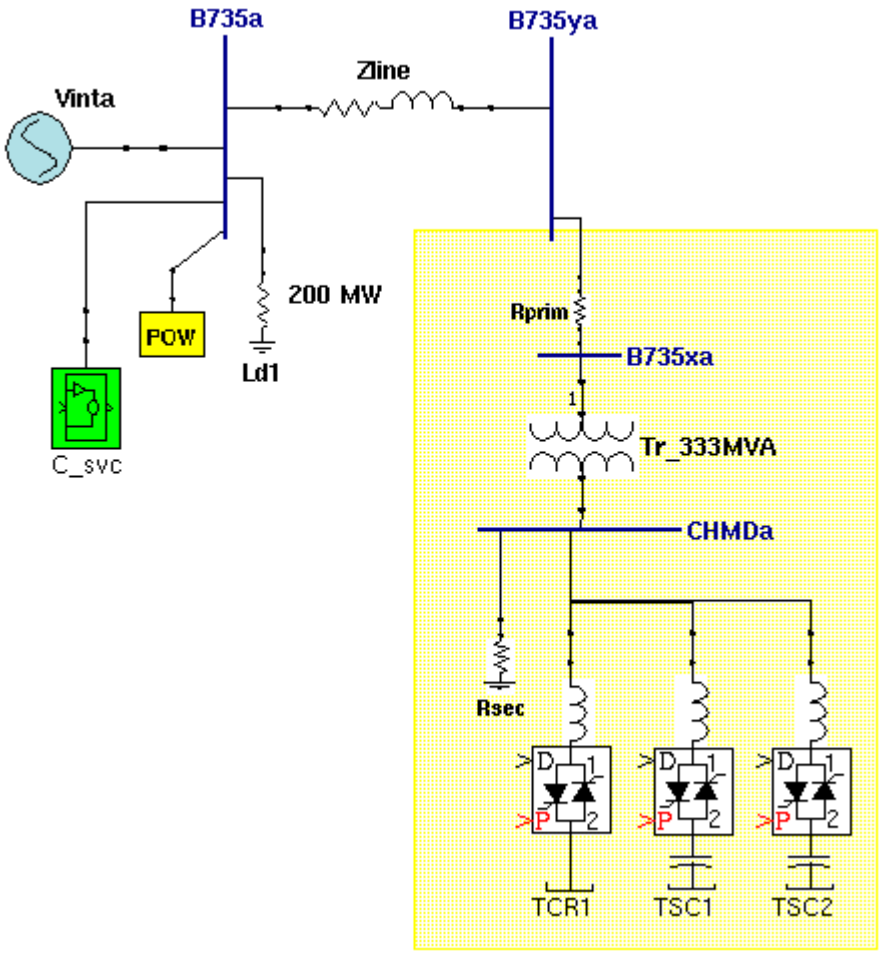


Figure 11 - 32 Test network for the static compensator

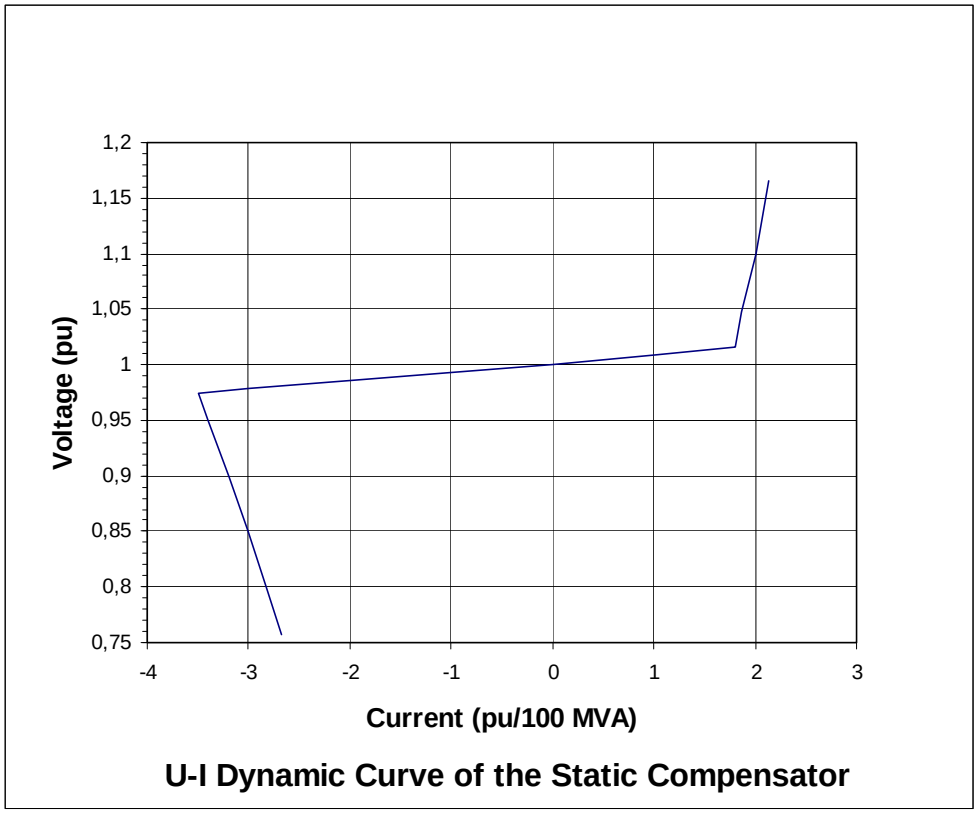


Figure 11 - 33 U-I dynamic curve of the static compensator